"Mischief" - Ultra Low Power Energy Harvesting PMIC (180nm SOI)

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Introduction

"Mischief" is an EI CFTD to develop a multi-source energy harvesting (EH), ultra-low power processing (ULP) PMIC to efficiently convert and manage power from Low Lux PV, Vibrational Energy Harvesting (VEH) types EMT, PZT, Electret Hybrid or Thermoelectric (TEG) source. It is a collaboration between **Tyndall and MCCI.**

Technology

The IC is being developed as a ***flexible ULP PMIC Platform IC*** on XFAB xt018 (180nm SOI)

ULP Mixed Signal Architecture:

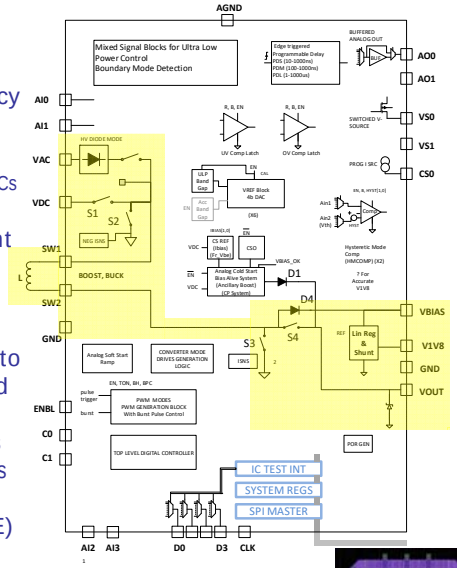
- 7 Advanced Asynchronous PWM Modes for 1st Valley Quasi Resonant 4-Switch Buck-Boost Topology
- Advanced ULP asynchronously triggered digital timers
  - 300MHz Clock and Digital Counter based
  - Current Starved Cap Charging and 20nA Comparator
  - New Delay Architecture for ULP Hi-Res Long Delays with Dynamically Clocked Comparator
- Fast high side current sensing comparator for SR switch drive
- 60nA fractional band-gap bias alive charge pump system
- SPI Master for Serial EEPROM Configuration

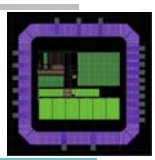
Status

Block schematics almost complete for 3 test chips. Tape-out Q1/Q2 2018

USPs:

- Highest efficiency from 1uW upwards.
  - (Marketplace ICs enter at 15uW)
- Lowest quiescent current (IQ ~200nA)
- Flexible Mixed Signal Platform to enable advanced next generation features such as PZT Synchronous Electric Charge Extraction (SECE)





Chip 1 of 3 test chips

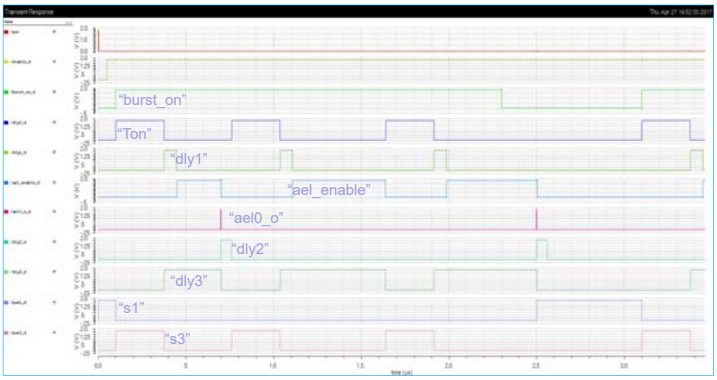
0.18 Micron Modular Trench Isolated SOI CMOS Technology

Multiple Asynchronous Quasi-Resonant PWM_MODES

- Mixed signal PWM modes for Inductor based Switch-Mode topologies
- Separate Switch Capacitor bias alive/cold-start

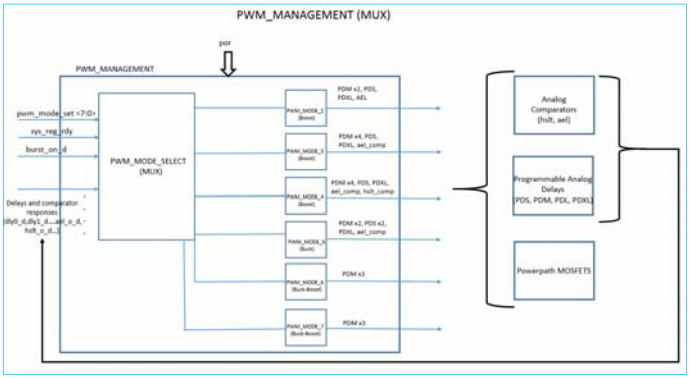
Example: PWM_MODE_2 (1st Valley Quasi-Resonant Boost)

Synthesized Asynchronous Verilog Simulation - AMS



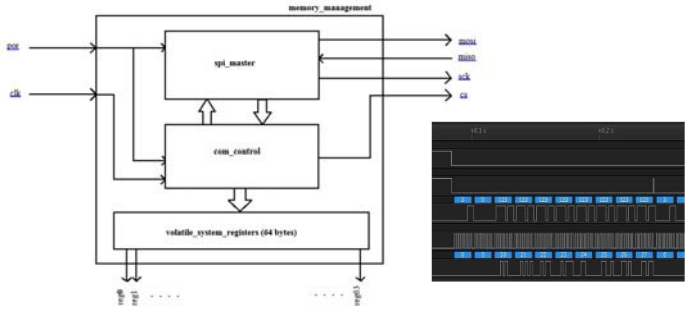
PWM_MANAGEMENT (PWM_MODE MUX)

- Digitally programmed block which manages triggered analogue delays, event comparators and control blocks specific to the selected mode



Synchronous SPI Block (MEMORY_MANAGEMENT)

- During the initial Power-Up sequence, a synchronous SPI master block running from a temporary low-frequency clock configures internal memory registers from an external EEPROM.



Hardware validated SPI data transfer using Digital Logic Analyser and Decoder using FPGA and Serial EEPROM Memory Chip

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