CFTD

This work has also been supported by Science Foundation Ireland (SFI) and is co-funded under the European Regional Development Fund under Grant Number 13/RC/207.

Energy Harvesting ULP PMIC for Smart Sensor Node

Enerharv 2018 – Power Management

Séamus O'Driscoll, Tim Daly, James McCarthy, Gerry McGlinchey, Ivan O'Connell, Michael Hayes

28th May 2018

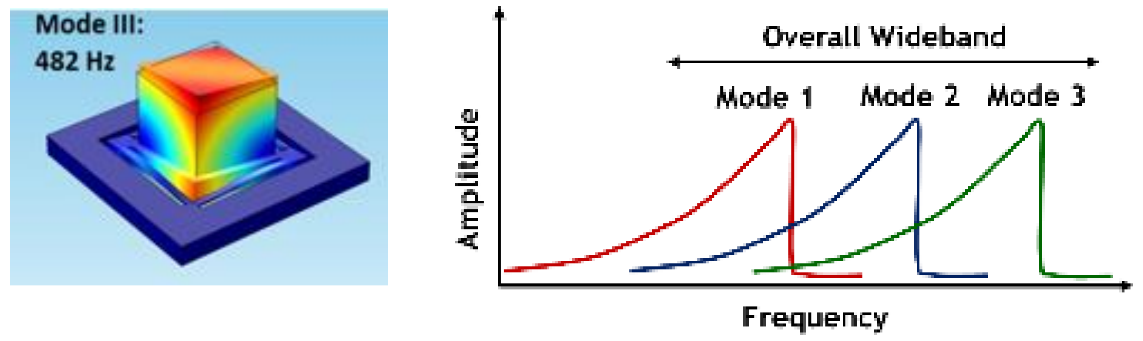
Tyndall National Institute
Institiúid Náisiúnta

EnerHarv 2018

On-Site Research Groups contributing to Energy Harvesting & PMIC Development

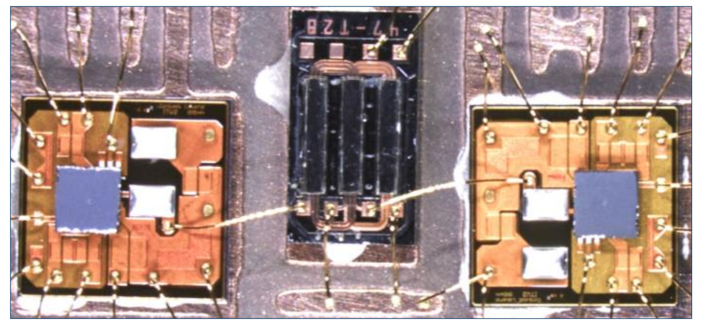
itOBO MOSYCOUSIS

ICT4EE Systems
(Energy Efficiency)



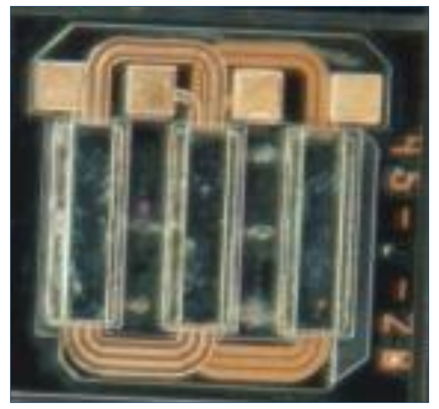
Vibrational Energy Harvester

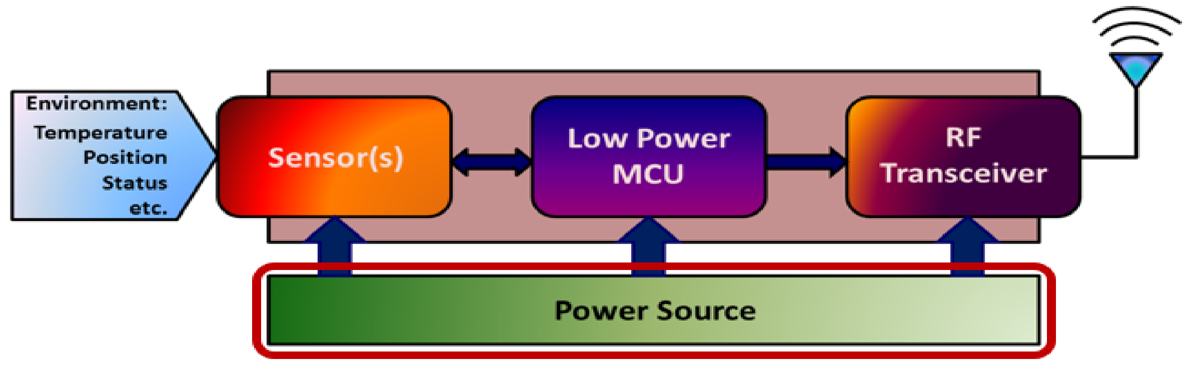
MCCI
Microelectronic Circuits Centre Ireland



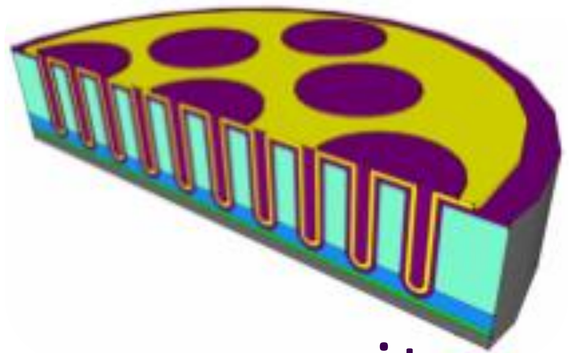
PWRSiP, PWRSoC

Materials
Structures
Magnetics on Silicon




Environment:
Temperature
Position
Status
etc.
Sensor(s)
Low Power MCU
RF Transceiver
Power Source

WSN

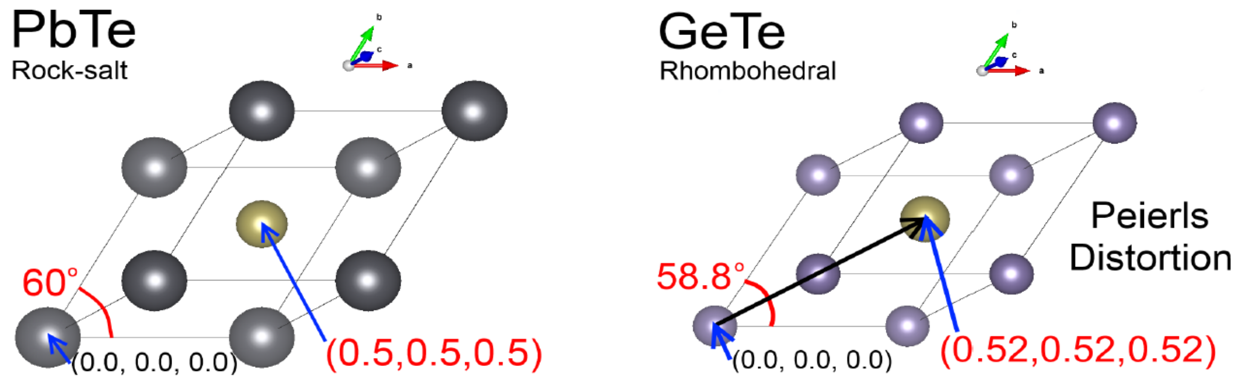


Solid State Supercapacitors

Solid State
Energy Cells

Material Model & Synthesis

Mix materials with slightly different atomic arrangements:


PbTe
Rock-salt
60°
(0.0, 0.0, 0.0)
(0.5,0.5,0.5)
GeTe
Rhombohedral
Peierls Distortion
58.8°
(0.0, 0.0, 0.0)
(0.52,0.52,0.52)

Integrated Power Systems and PMICs

Integrated Systems Design

UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

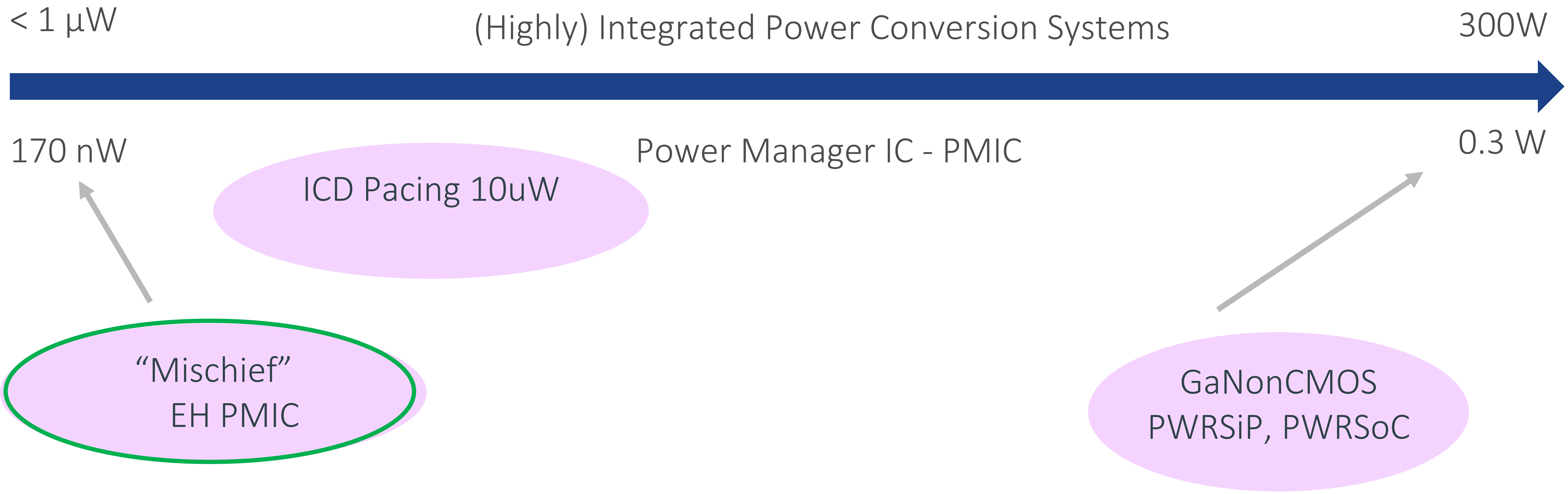
Ireland's European Structural and Investment Funds Programmes 2014-2020
Co-funded by the Irish Government and the European Union

European Union
European Regional Development Fund

Power Conversion & PMIC at Tyndall:

Smart Sensor Power
Ambient Energy Harvesting
Implantable Power
Couplers, EMT

DC-DC: POL, VR, SoC
Switch Mode Inductor or Hybrid Topology
Advanced Magnetic Component Designs 1-100M
BEOL Wafer Scale RDL based Thin Film Magnetic Materials,
Substrate Embeddable



< 1 µW

(Highly) Integrated Power Conversion Systems

300W

170 nW

Power Manager IC - PMIC

0.3 W

ICD Pacing 10uW

“Mischief”
EH PMIC

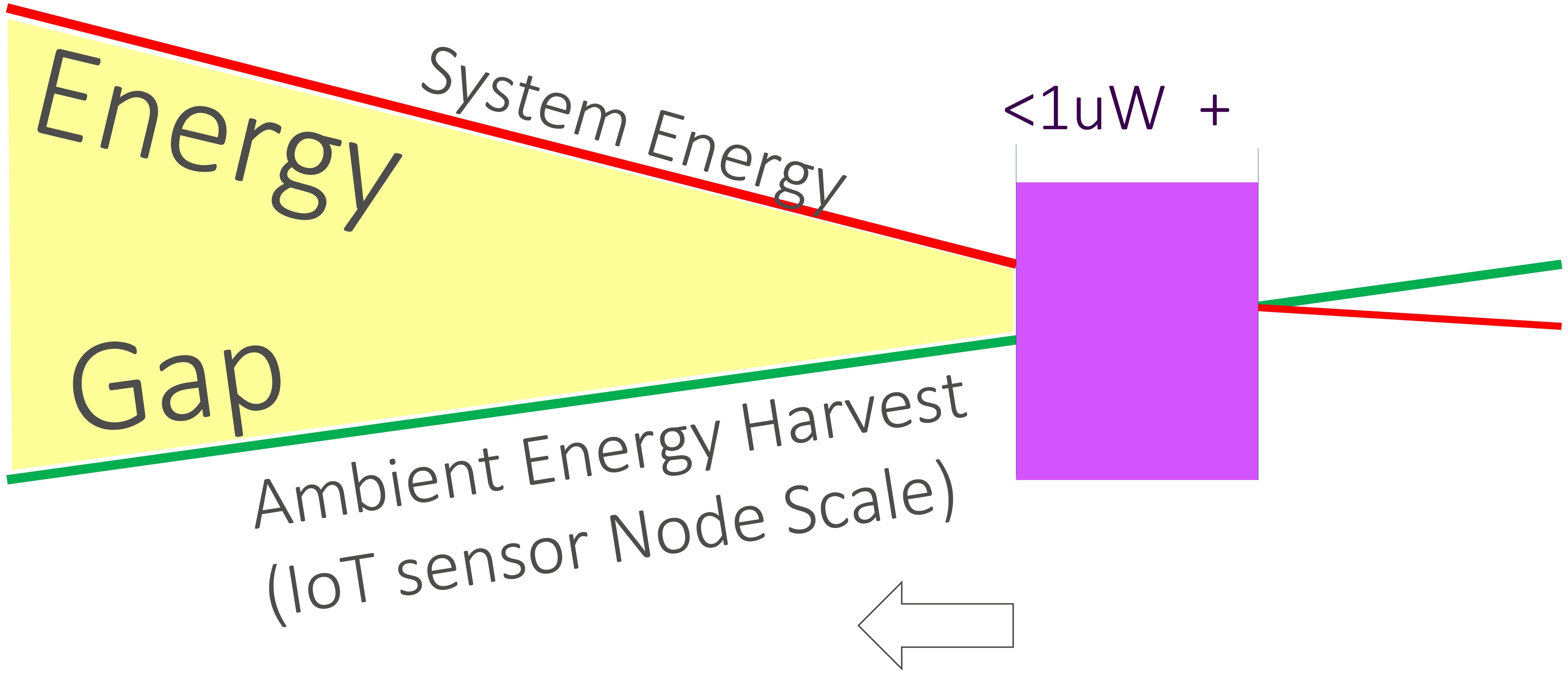
GaNonCMOS
PWRSiP, PWRSoC

Ultra Low Power (ULP) PMICs

Low Bandwidth and Low Average Data ***"battery-less"*** (maintenance-free) systems

Or

Battery Life extension to 25+ years



Energy Gap

System Energy

<1uW +

Ambient Energy Harvest (IoT sensor Node Scale)

Power and Energy Data points

Short-range (BLE) Wireless SoC
Wearables - 1µA Idle with 32kHz & RTC
~2.4uW average for radio for heart rate profile – 4bytes/s for 1h/day

Ocular (retina) implant system @ IDD=50nA

Hearing Aid DSP - <100uA/MIPs

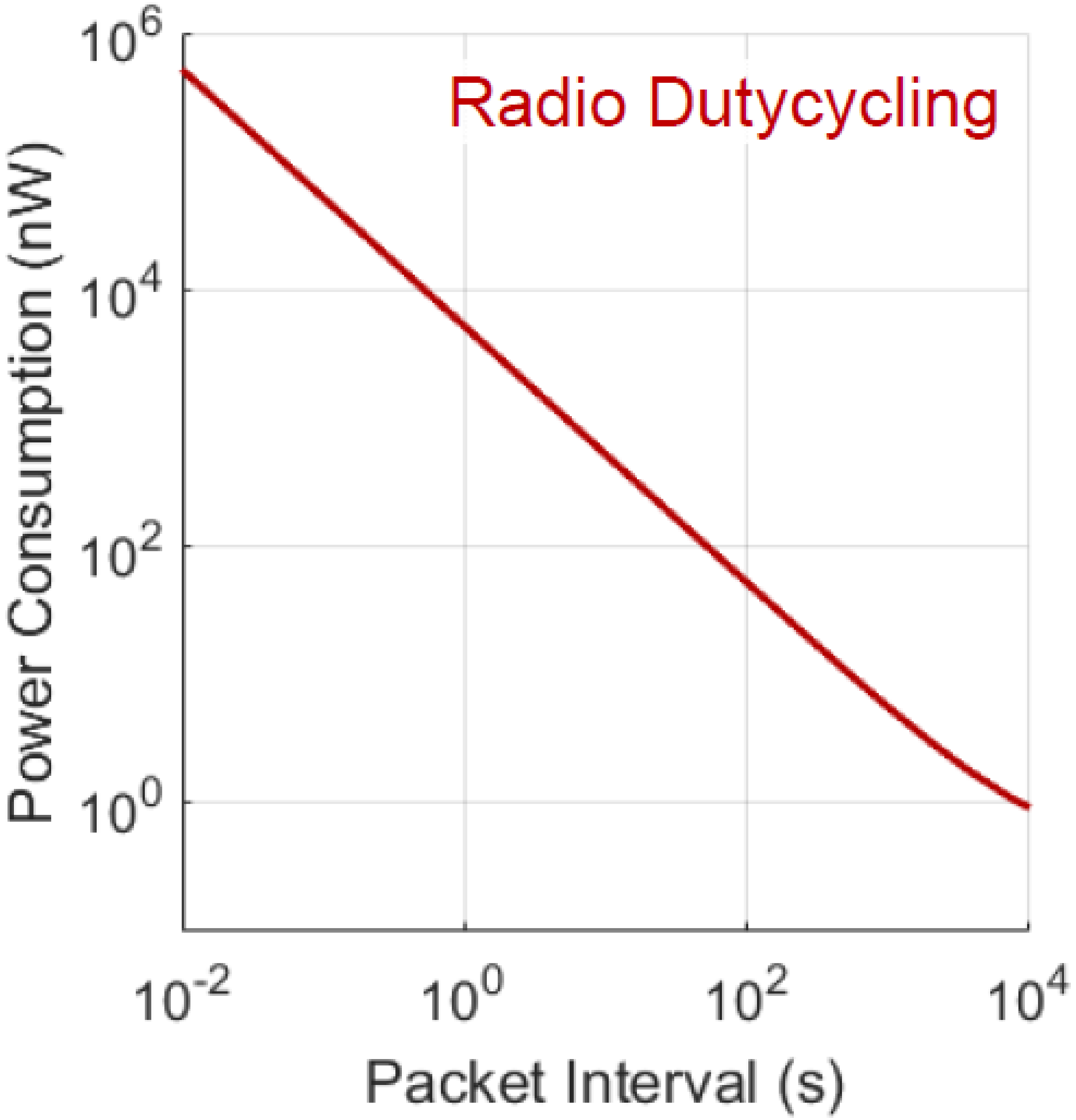
SOA Technology Solid State Storage on 1.5mm X 1.5mm die will provide ~15µW.h (10µm layer)

ICD Pacing Circuits 1-10uW

ADuCM4050 Signal Processor 40µA/MHz active & 680nA hibernate

Wide Dynamic Range & Heavily Duty Cycled Loads and Sources

Solar cells
- 100klux outdoors
- 10lux indoors
- Upto 10^4 dynamic range of available power
- sub-nA with low area cells



- We measure 10 lux under a bench, 300 lux in “brightly lit” room
- Solar Cell Dynamic Range 1×10^4 [Paidimarri et al, ISSCC ‘17]
- Radio has 7.6×10^7 Dynamic Range [Paidimarri et al, ISSCC ’15]

Control Silicon - ULP Wireless System Node

PMIC
Harvested Energy Conversion
Energy Storage Management
Battery Management
Regulated Voltages for the System
System Controller
Sensor Interface
Radio
RF

- The PMIC is currently generally a discrete IC
- But at ULP level the smart sensor node ***ideally requires a very high level of integration***

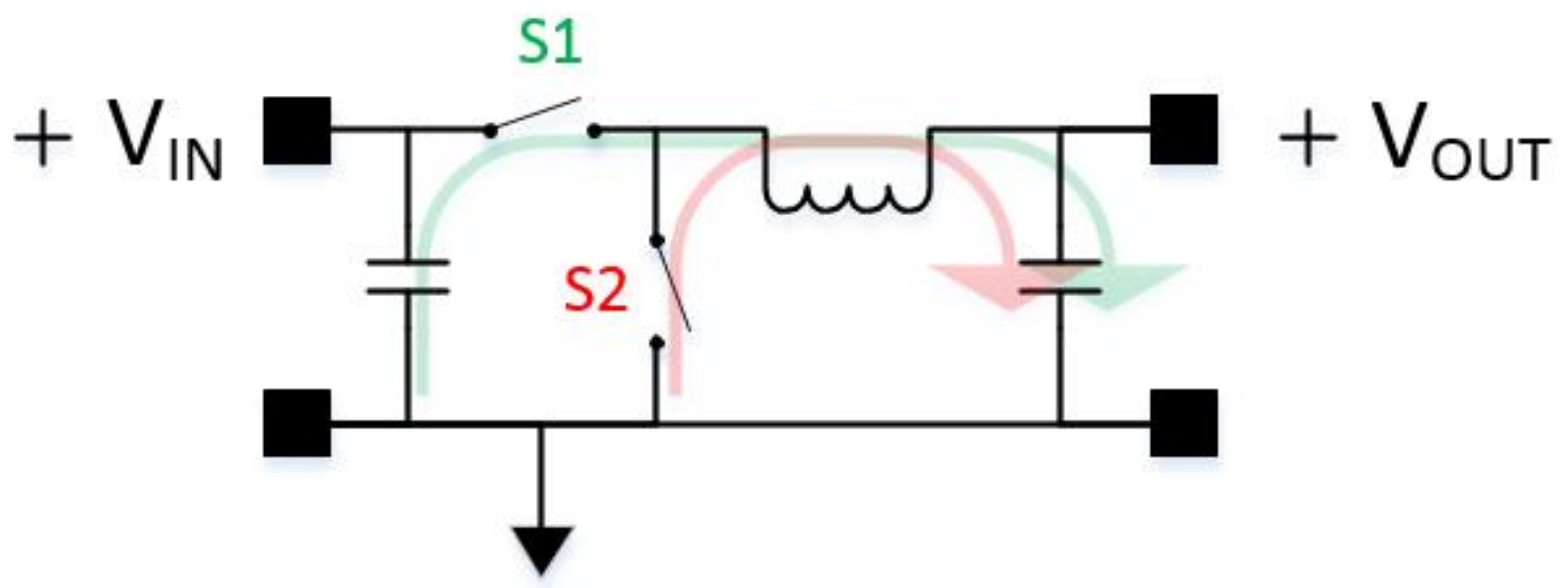
  PMIC Voltages, Silicon Requirements and Control are very compatible with radio

  Mixed-signal sensor interface circuits are very similar to those for energy source interaction and power control

  Outer loop (tertiary) power control should ideally share resources with the system (host) controller.

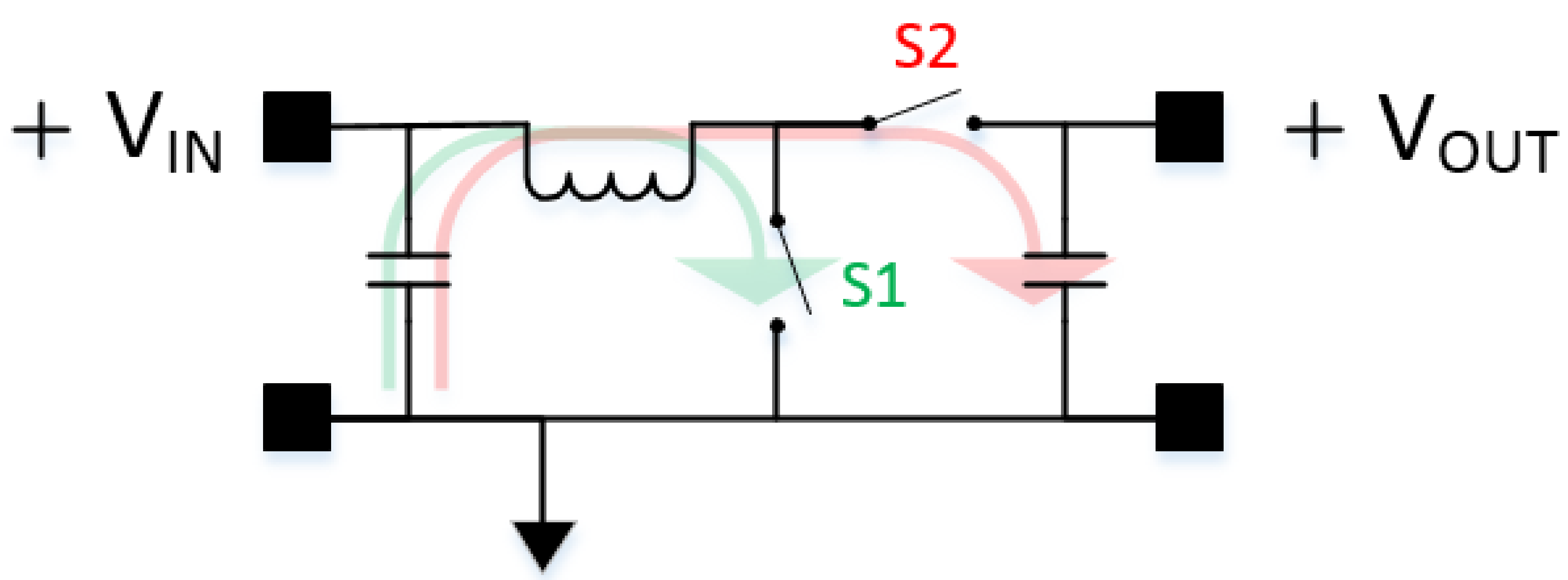
- Accordingly “Mischief” represents flexible, mixed-signal, ULP-PMIC *platform IP offering*

Switch Mode Inductor Topologies


+ V_{IN}
S1
S2
+ V_{OUT}

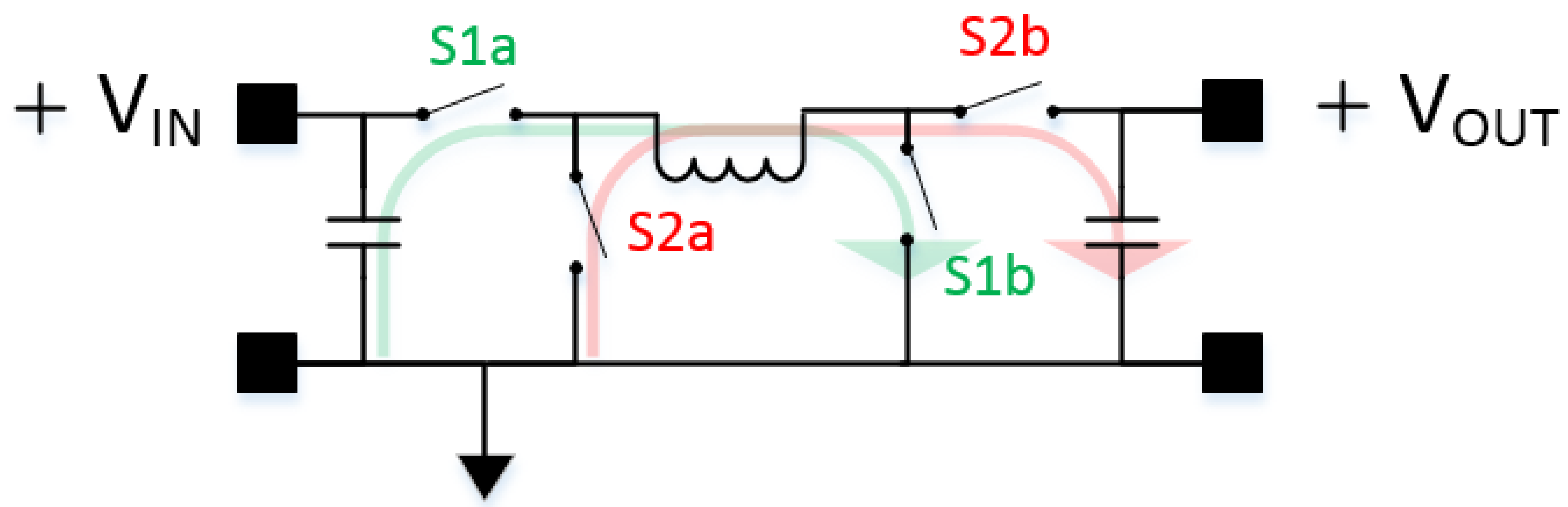
Buck

$V_{IN} > V_{OUT}$


+ V_{IN}
S2
S1
+ V_{OUT}

Boost

$V_{OUT} > V_{IN}$


+ V_{IN}
S1a
S2b
S2a
S1b
+ V_{OUT}

Buck-Boost

V_{OUT} <,> V_{IN}

Inductors are beautifully voltage compliant

Buck or Boost are more efficient than Buck-Boost

Inductors are large when looking for small Δi

PMIC Platform IP Development Goals

- Extend to sub - 1µW for emerging MICRO, MESO and MESO

  Emerging Smart Sensor Node Controllers such as ADuCM4050 (40µA/MHz active, 680nA in hibernate mode, rapid start)

- Control flexibility to maximise energy transduction, energy storage and full-system energy efficiency

  - for a variety of energy harvester types: PV, TEG, Piezo, Electromagnetic and Electret

- Bring advanced intelligent control to the space (digital and mixed-signal)
- Leverage the benefits of digital assisting analog for low quiescent current PMIC circuits and references
- Create flexible solution IP to address power management challenge for IoT devices
- Cater for multiple system voltages, multiple input-output ratios and extend input voltage range
- A lot of niche smart sensor applications will require dynamic and intelligent fit with:
  - the application environment
  - the sensor
  - the radio
  - the energy source nature, type, MPPT, impedance
  - the storage

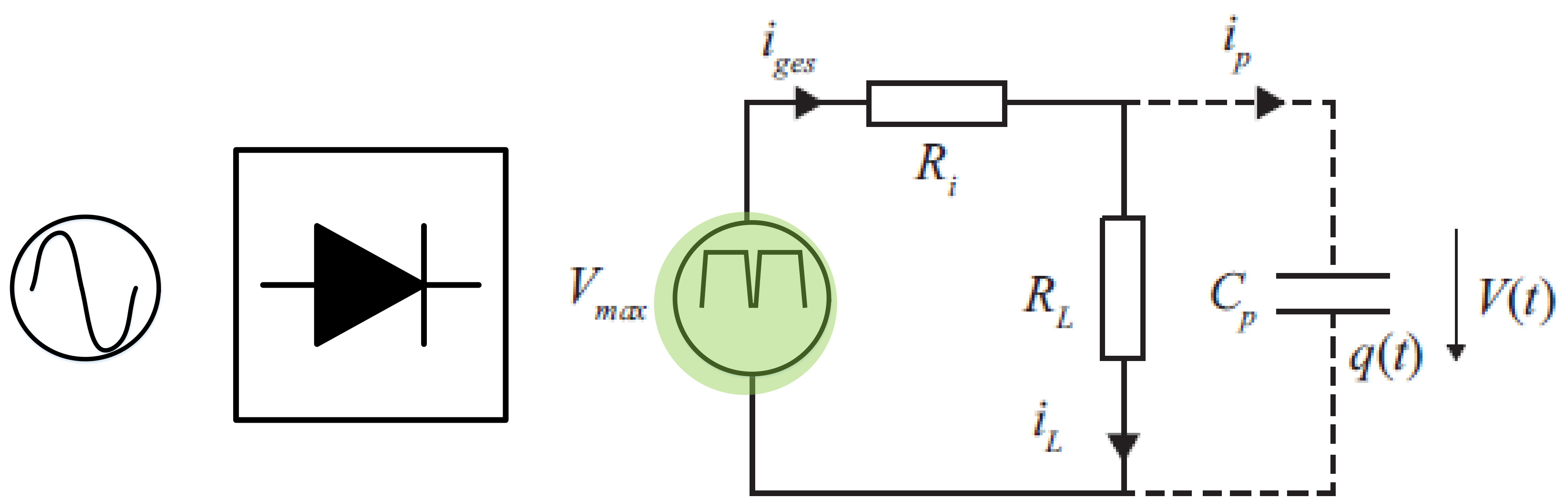
Enabling High Value, Novel, Next Generation Features

Digitised outer loop power/current set points for MPPT will enable features such as **performance monitoring of source and storage**

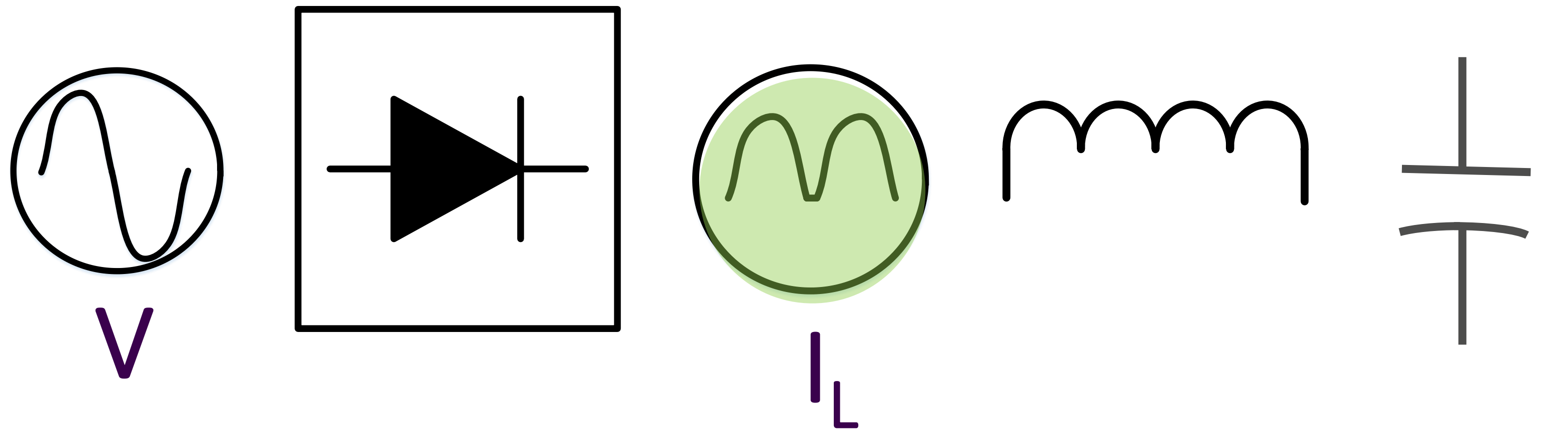
Charge profile tuning to suit **emerging battery chemistries**

VEH is AC and will be by Active Rectifier & DC-DC or Power Factor Improvement or Hybrid

Piezoelectric, electret devices tend to be current source in nature
Electromagnetic transduction tend to be voltage source in nature



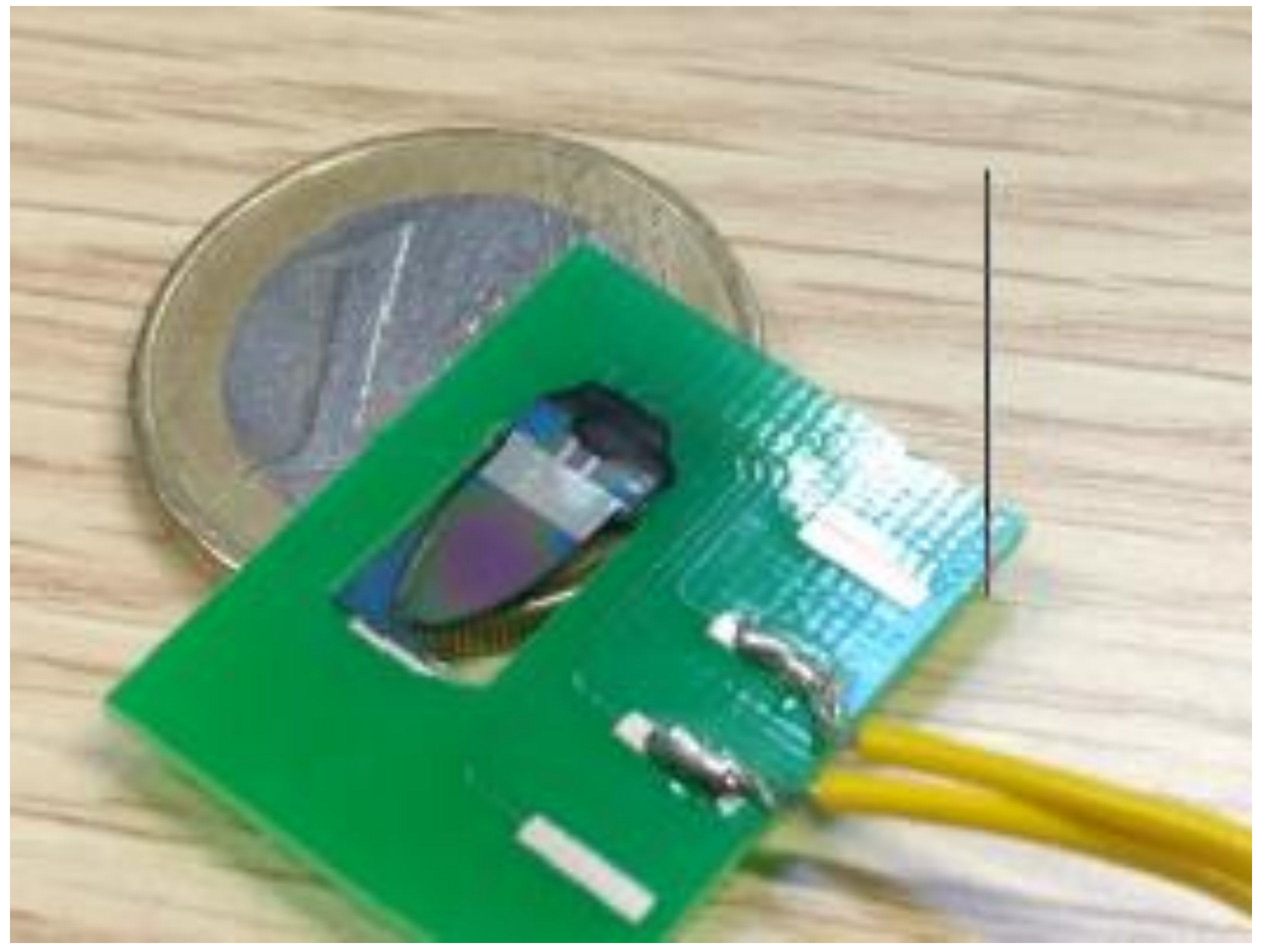
Active Rectifier

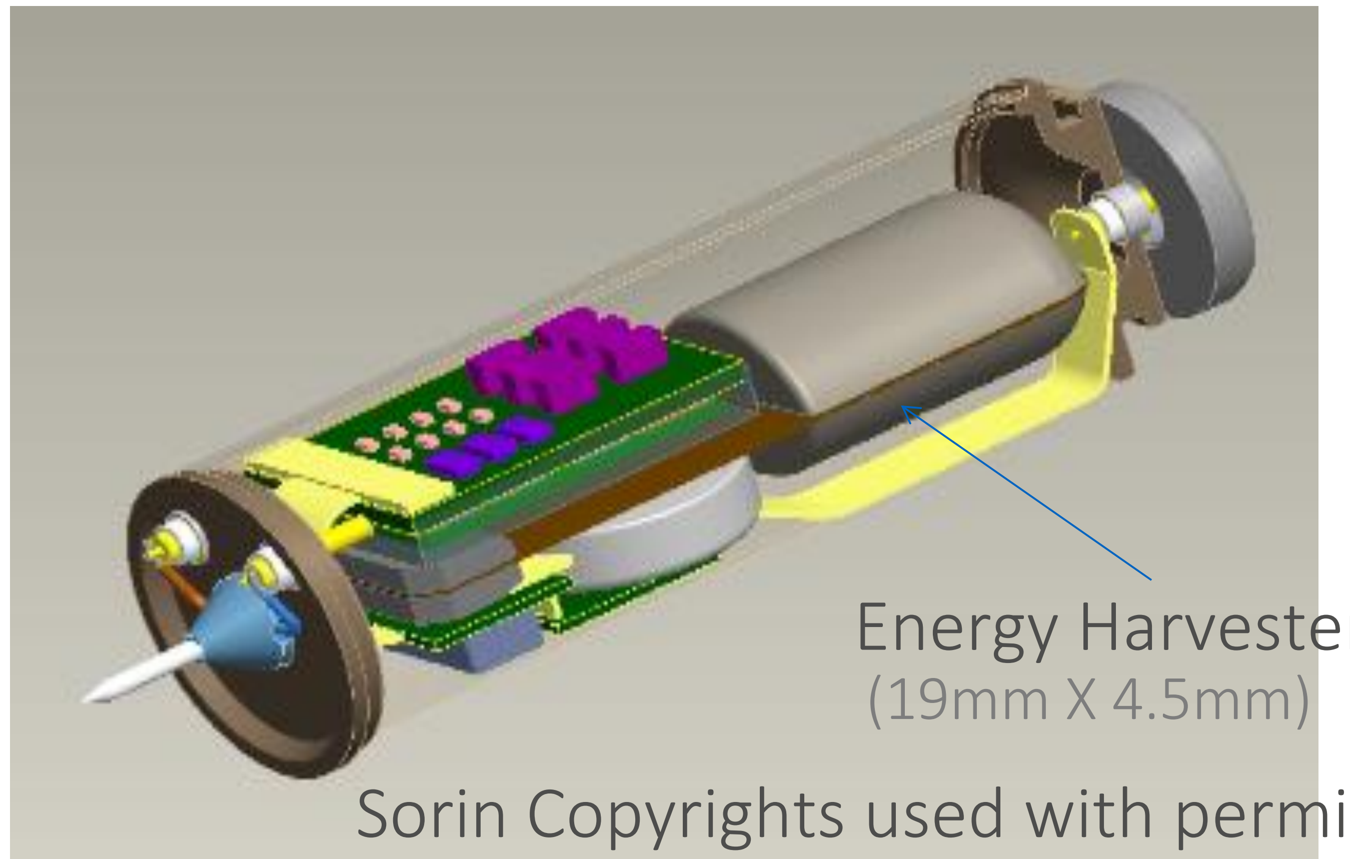


Boost to HV
“Bulk”
Storage
Capacitor

Power Factor Improvement

ULP PIEZO Research – AlN Piezo Harvester





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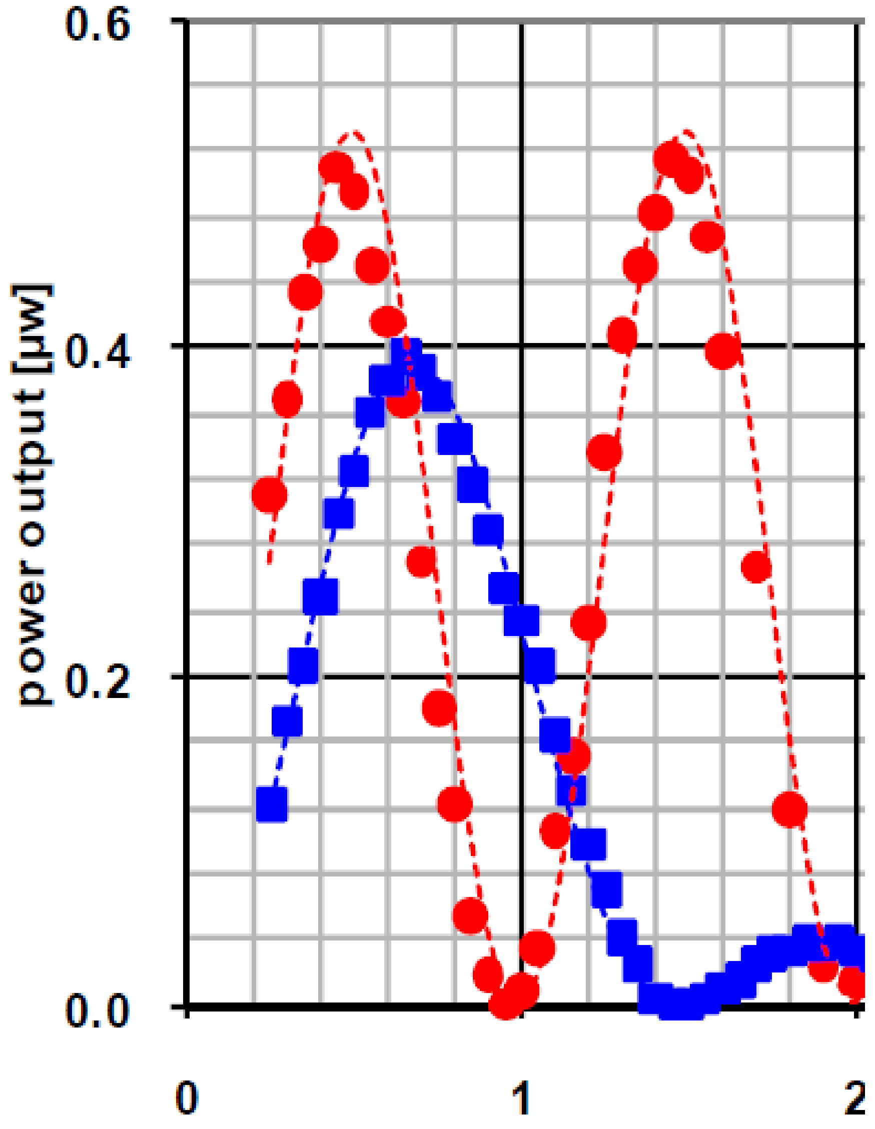
www.themanpowerproject.eu



Elfrink et al. 2010

Blue: Shock induced off resonance

Red: At resonance

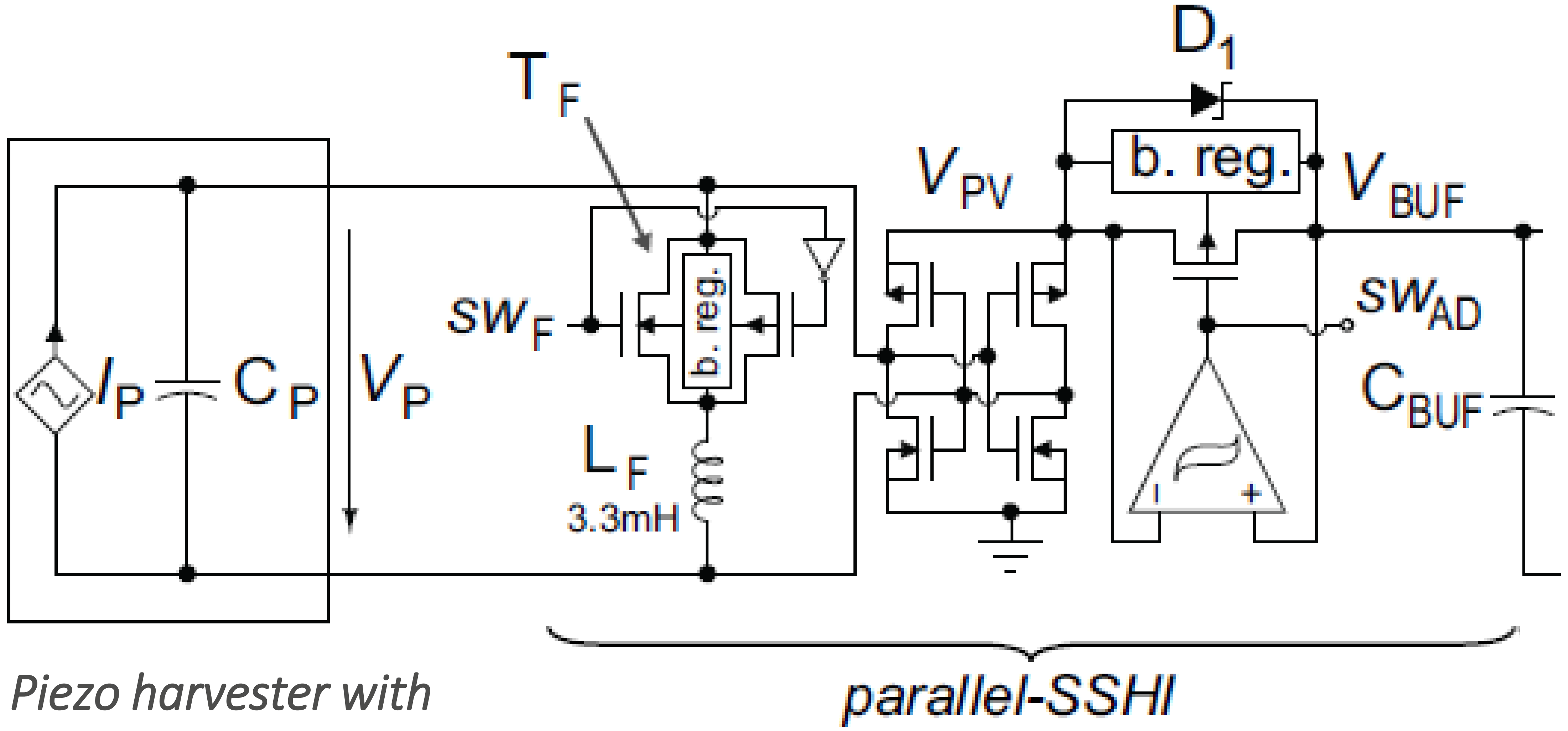
Leadless implantable – Tyndall created the Piezo harvester – double cantilever
~3uW (1-10V) average power operating at 60 bpm, fits inside a commercial leadless pacemaker.
Off-resonance based on impulse acceleration method – MEMs compatible process

Substantial further improvements are possible and mixed signal control will add value

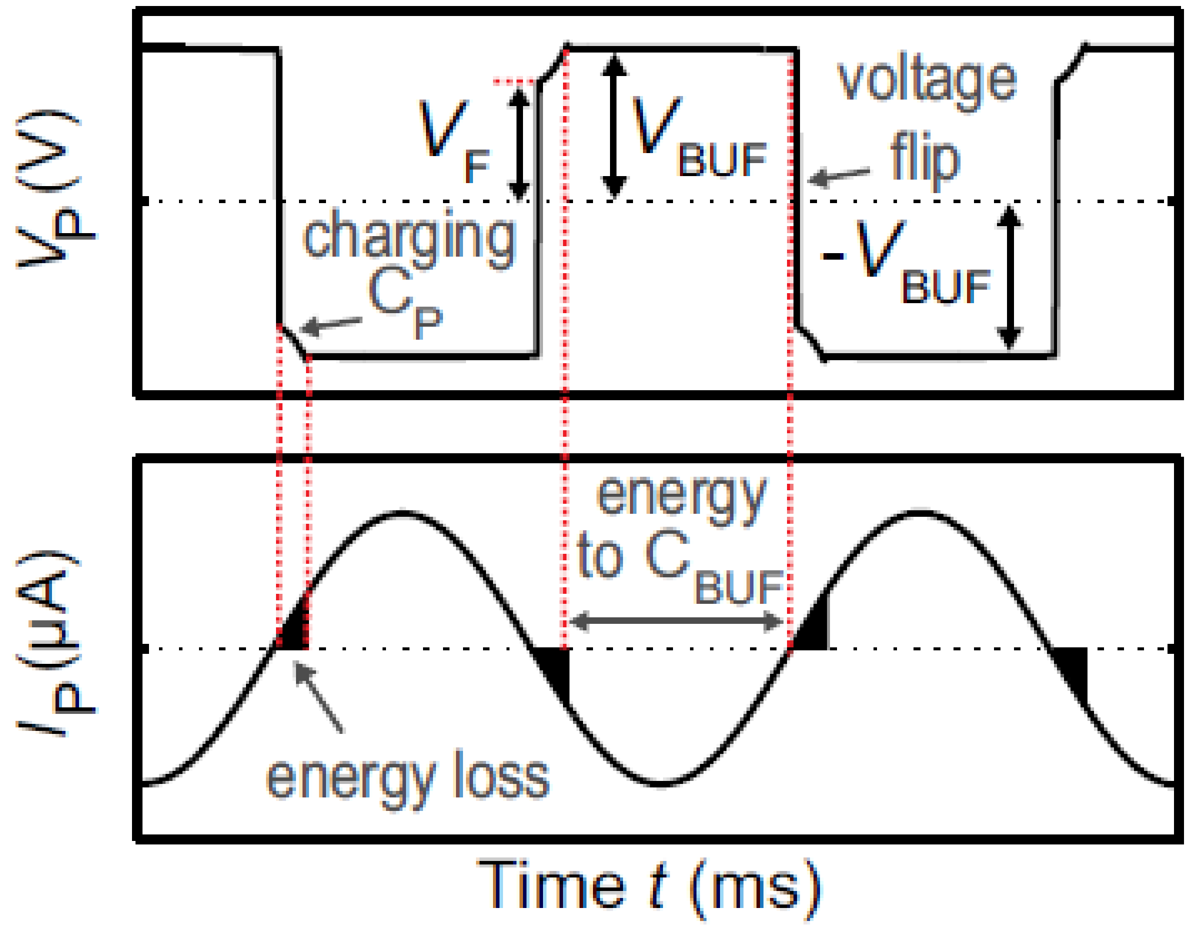
Maximise energy extraction during single shock excitation, as an example.

Piezo – Energy Extraction at Mechanical Vibration Frequency from a Capacitive Source

- At the vibration frequency (Ω_M) – facilitates ULP
- A quickly evolving variety of Active Rectifier, Conduction Angle Extension (Bias Flip, Parallel Synchronous Switch Harvesting on Inductor (P-SSHI)) or other Synchronous Charge Extraction (SECE) techniques.



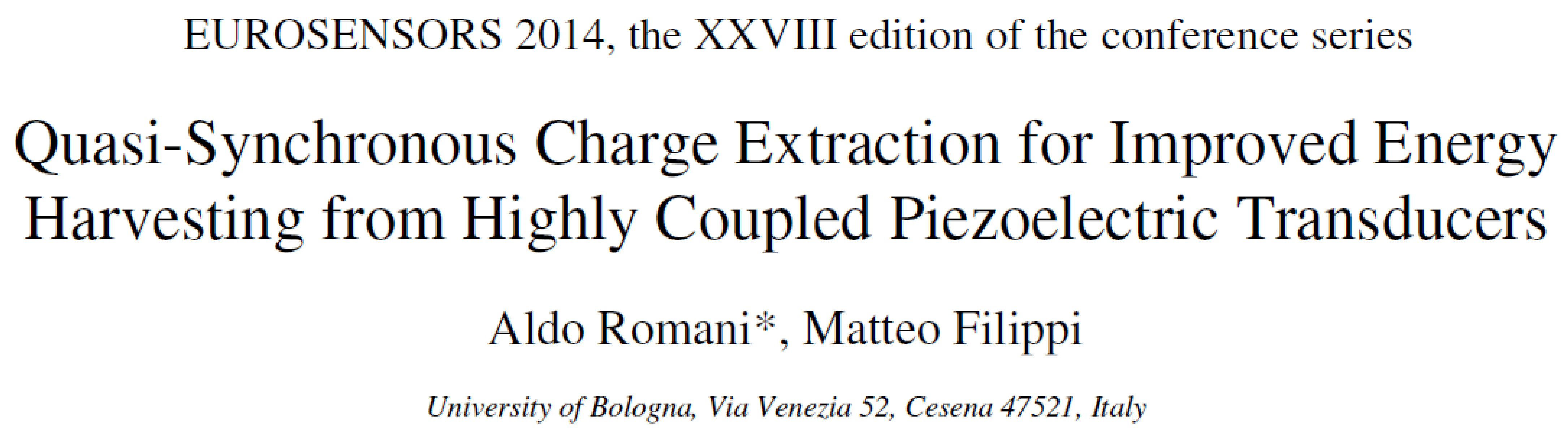
Piezo harvester with self capacitance, Cp



Current Source Generator results in Square Wave Voltage determined by MPPT Control of DC Voltage after the rectifier

"A 4μW-to-1mW Parallel-SSHI Rectifier for Piezoelectric Energy Harvesting of Periodic and Shock Excitations with Inductor Sharing, Cold Start-up and up to 681% Power Extraction Improvement", Daniel A. Sanchez et. al., ISSCC 2016

SECE Piezo Harvesting Circuit Example

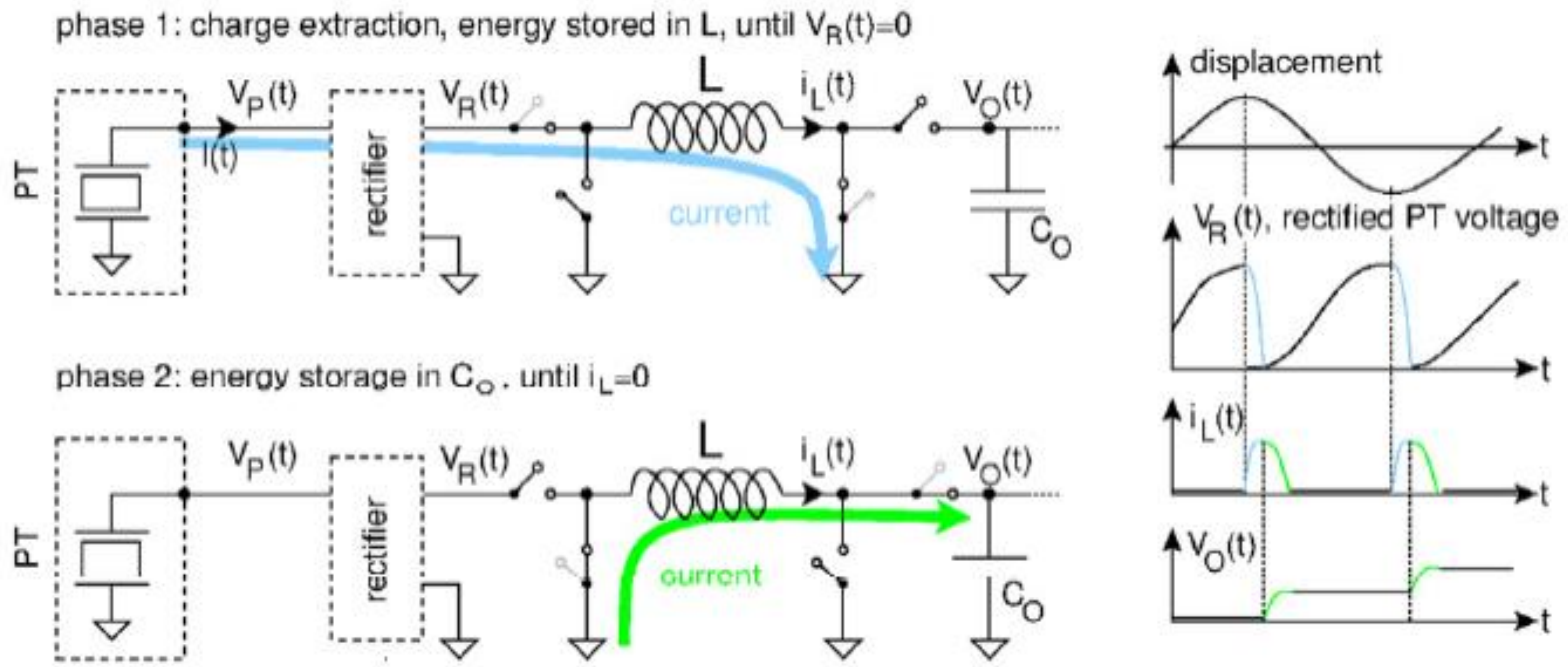


EUROSENSORS 2014, the XXVIII edition of the conference series

Quasi-Synchronous Charge Extraction for Improved Energy Harvesting from Highly Coupled Piezoelectric Transducers

Aldo Romani*, Matteo Filippi

University of Bologna, Via Venezia 52, Cesena 47521, Italy


phase 1: charge extraction, energy stored in L, until $V_R(t)=0$
PT
$V_P(t)$
$i(t)$
rectifier
$V_R(t)$
L
$i_L(t)$
$V_O(t)$
current
C_O
phase 2: energy storage in C_O, until $i_L=0$
PT
$V_P(t)$
rectifier
$V_R(t)$
L
$i_L(t)$
$V_O(t)$
current
C_O
displacement
t
$V_R(t)$, rectified PT voltage
t
$i_L(t)$
t
$V_O(t)$
t

This is a Buck-Boost Circuit operated synchronously with mechanical vibration to resonantly (efficiently) extract charge from the piezo capacitive source

All of these harvesting circuits benefit from:

- MPPT
- Analog Event Driven State Machines
- Digital Timing Curcuits
- High Speed Low Threshold Comparators

Mechanical and Electrical Co-Design VEH

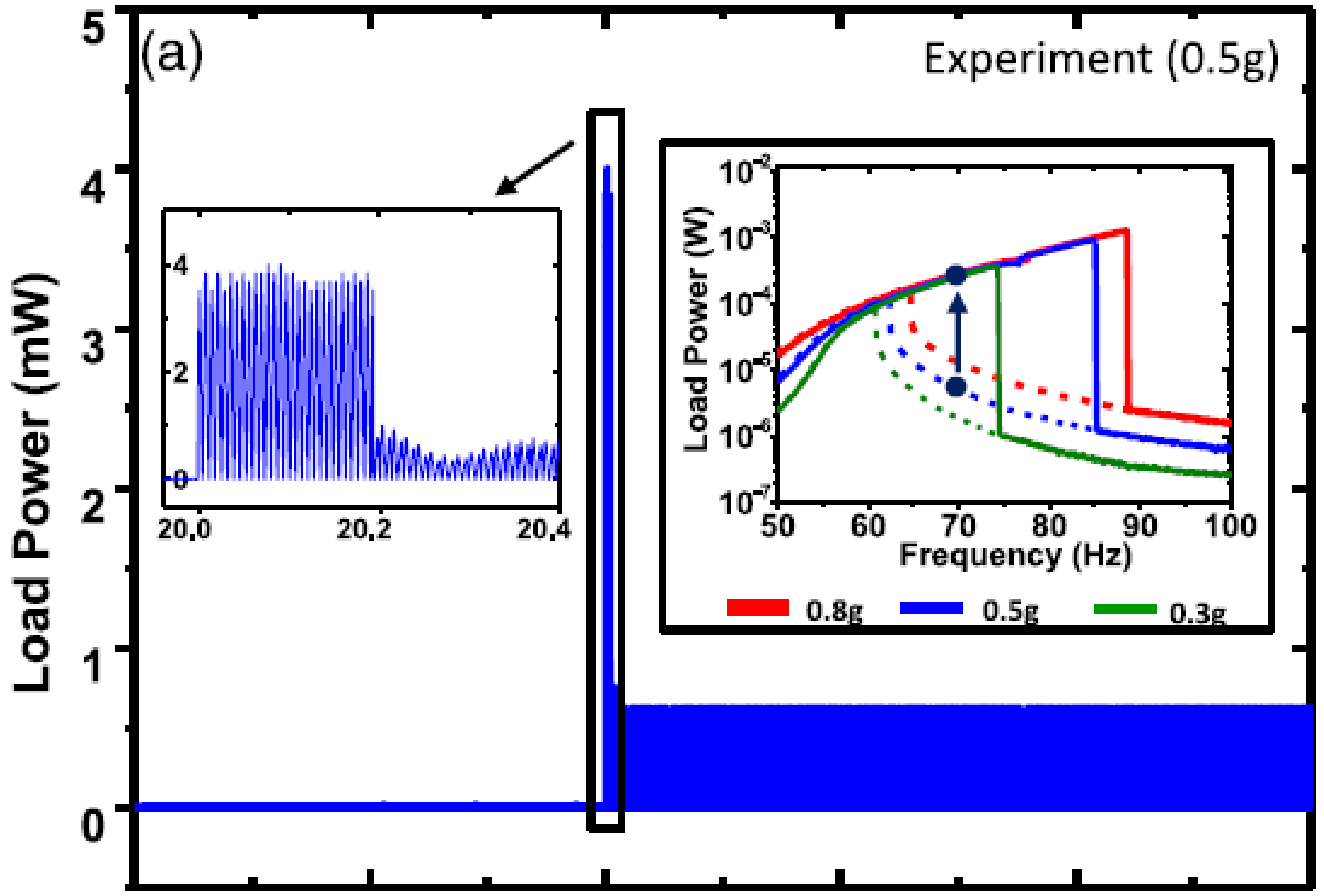
- **Mechanical Non-Linearities** added in transducer design +
- **Non-Linear Electrical Stimuli** to maintain high energy branch resonances
-

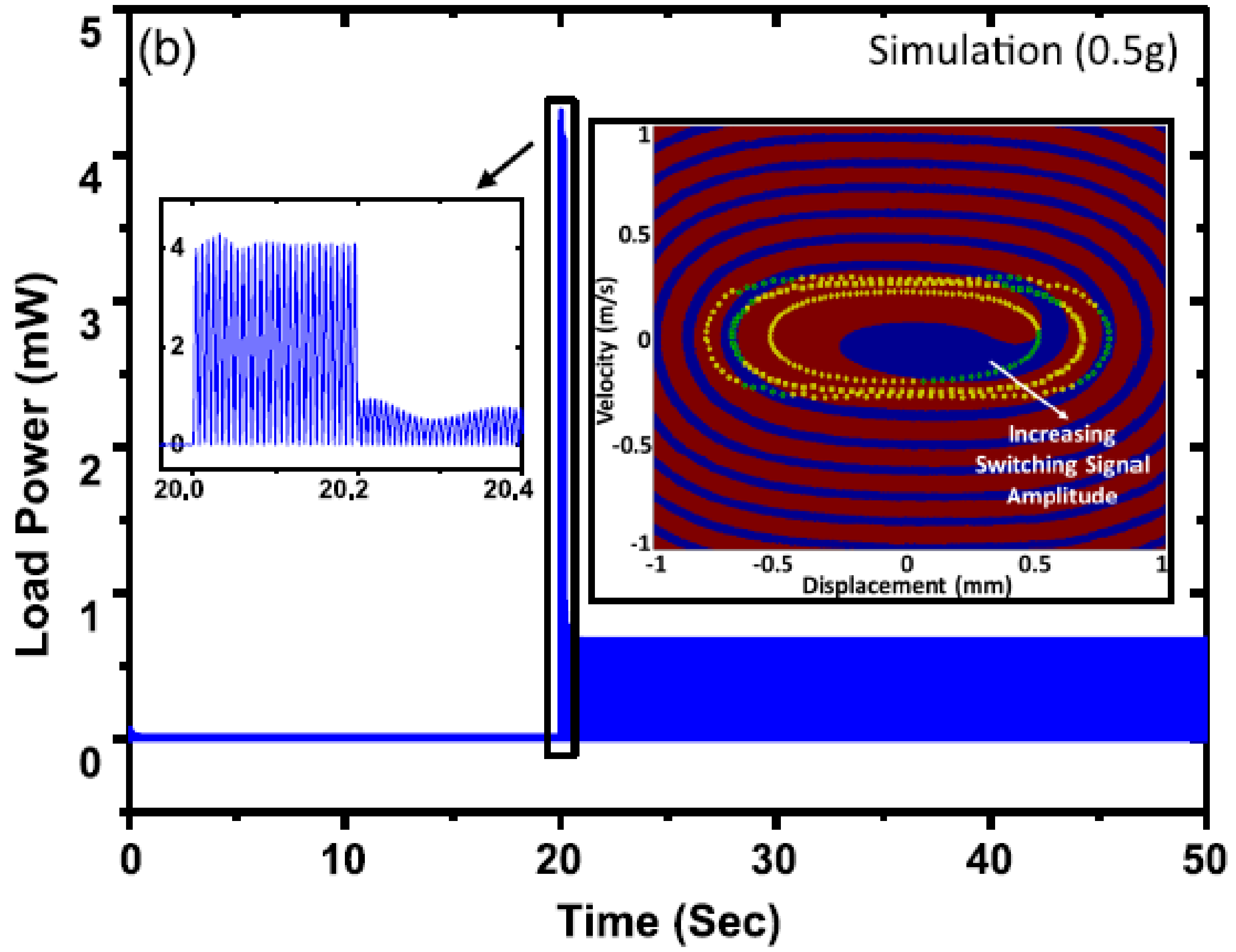
- Design for high reliability involves advanced packaging design
  - *Signal interaction, such as displacement, strain measurement*
  - *Electrical techniques to increase reliability*

'**'Surfing the high energy branch of nonlinear energy harvesters'**, D. Mallick, S. Roy, Phys. Rev. Lett., week ending 4 NOVEMBER 2016, claim 32 X

Example for Electromagnetic VEH

There are analogous techniques for Piezo under review by IEEE MEMS





Platform Circuit Design Philosophy

- **Lowest Quiescent Current Blocks**, in combination with:
- **Optimised Energy Transfer per Cycle**
  - Frequency scalable or as required energy cycle transfer
  - Efficient and Linear over wide dynamic range
  - Burst Mark-Space duty cycling and optimum cycles per Burst Mark

- **Control functionality on demand – Control power ∝ burst frequency**

- **Inductor based Switch Mode**
  - Efficient at processing high energy per cycle
  - Inductors are extremely compliant for wide voltage range
  - *Drawback is that large L value and low DCR (high RMS) is required*

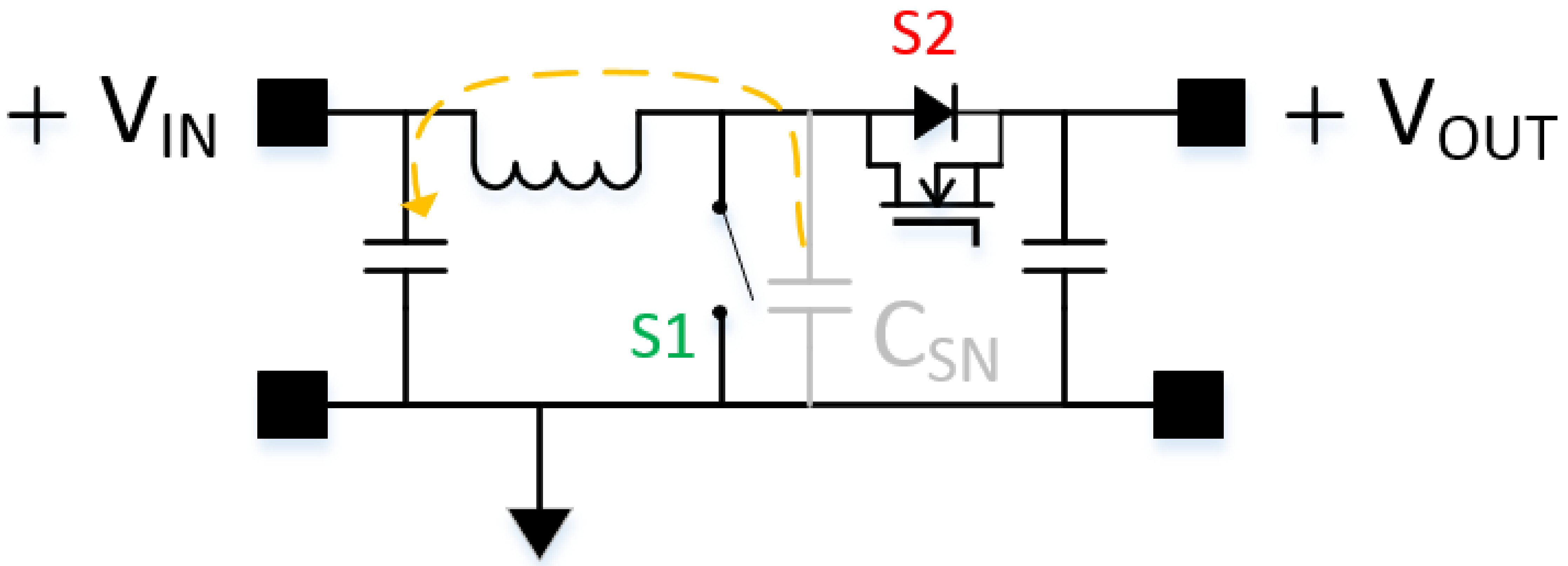
    *=> "very large" 22uH+ inductor – **4 x 4 x 1.8 mm (typical) size!***

- **Buck or Boost** (Buck-Boost Capability) for conversion to **multiple system voltages**
  - Time interleaving modes allows maximisation of efficiency and possible direct conversion to multiple system voltages

- Very low Switching Loss for **high frequency**
  - Quasi Resonant **(QR)** Switching achieves Zero Voltage Switching **(ZVS)** on Boost Switch or Buck Control Switch

- **SPI** Configurability

Quasi-Resonance Switching for (partial) ZVS

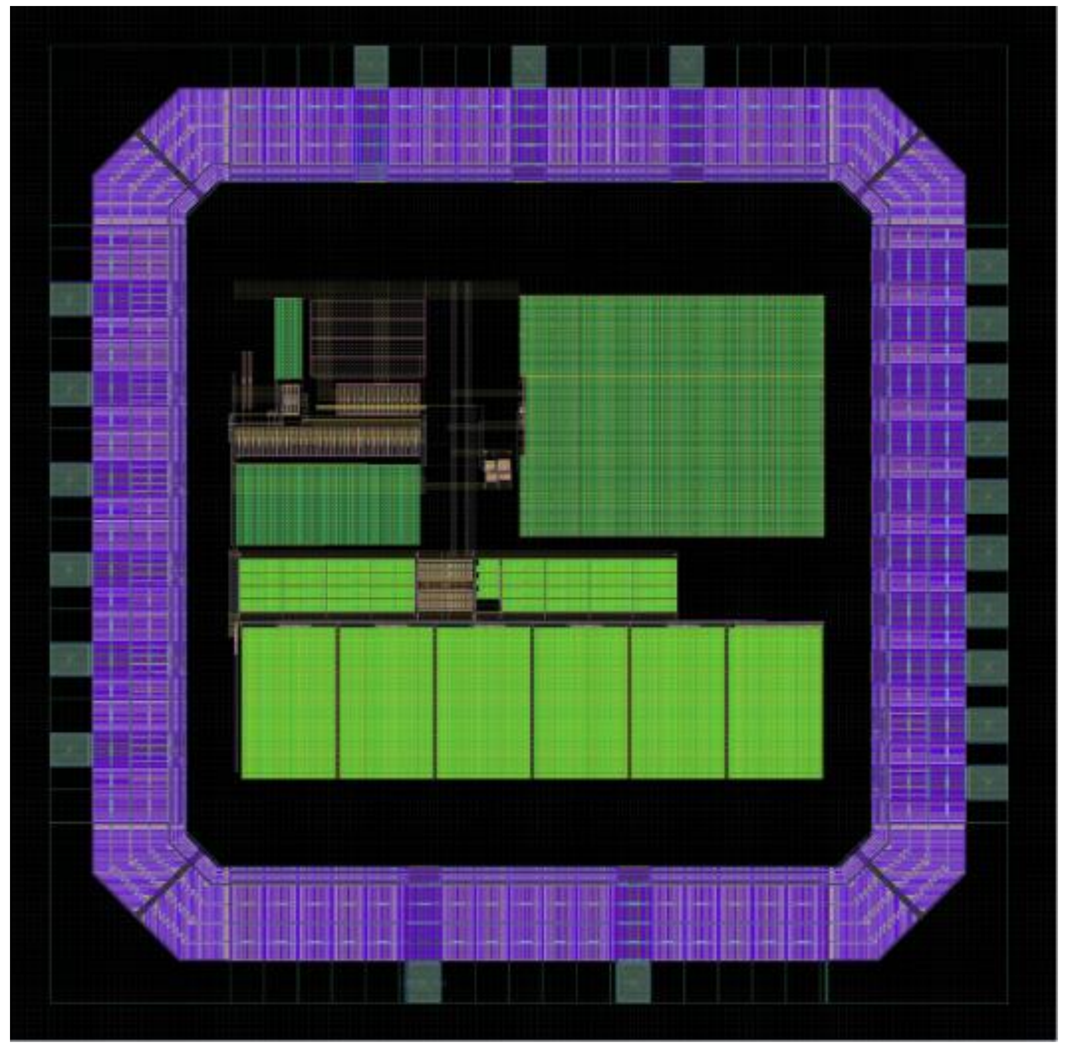


- Resonantly ring down voltage on Switch Node parasitic capacitance, C_{SN}, (after S2 body diode recovers)
- Recover this into source
- Enables ZVS for lower loss
- Enables higher switching frequency, smaller size/cost

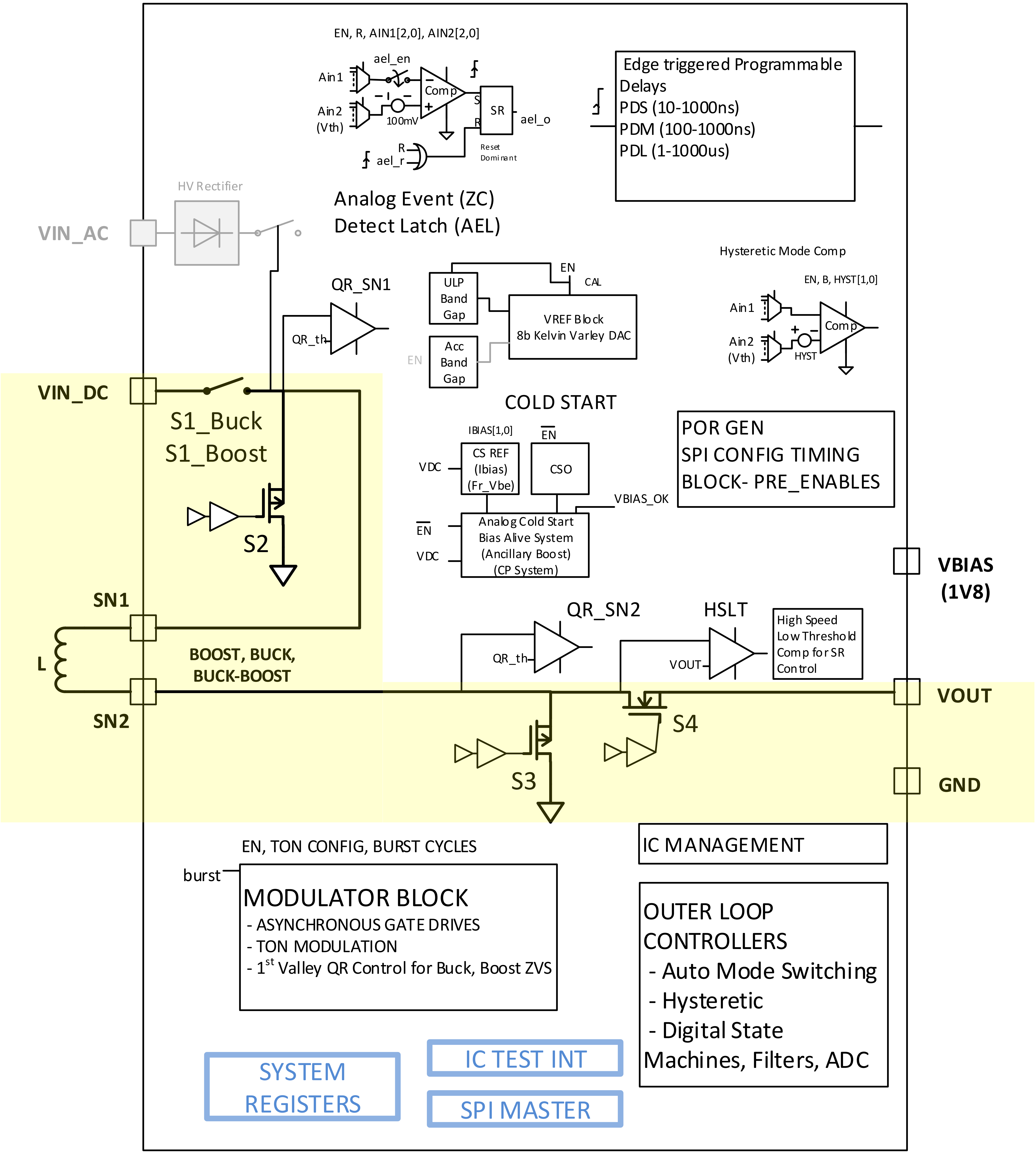
IC Process & Development Status

0.18 Micron Modular Trench Isolated SOI CMOS Technology

- **Process**: XFAB 180nm
  - Automotive, Medical and -40C-175C
  - Power, NVM & SOI options
  - High Res Poly
  - 125Kgates/mm^2
  - Low Sp.Ron Devices
  - 10V – 200V SuperJunction DMOS
- **3 Test Chips @ Top Level Schematic**
  i. COLD START/ BIAS ALIVE – Layout & DRC Clean
  ii. POWER PATH & DRIVERS – Top Level Sims
  iii. Full Chip *excluding* advanced outer control loops (hysteretic only)
    - – Synthesised Verilog & Top Level Sims
- MATLAB based *PMIC System* **Design Space Exploration**
  - Complete MATLAB models match top level Cadence Simulations



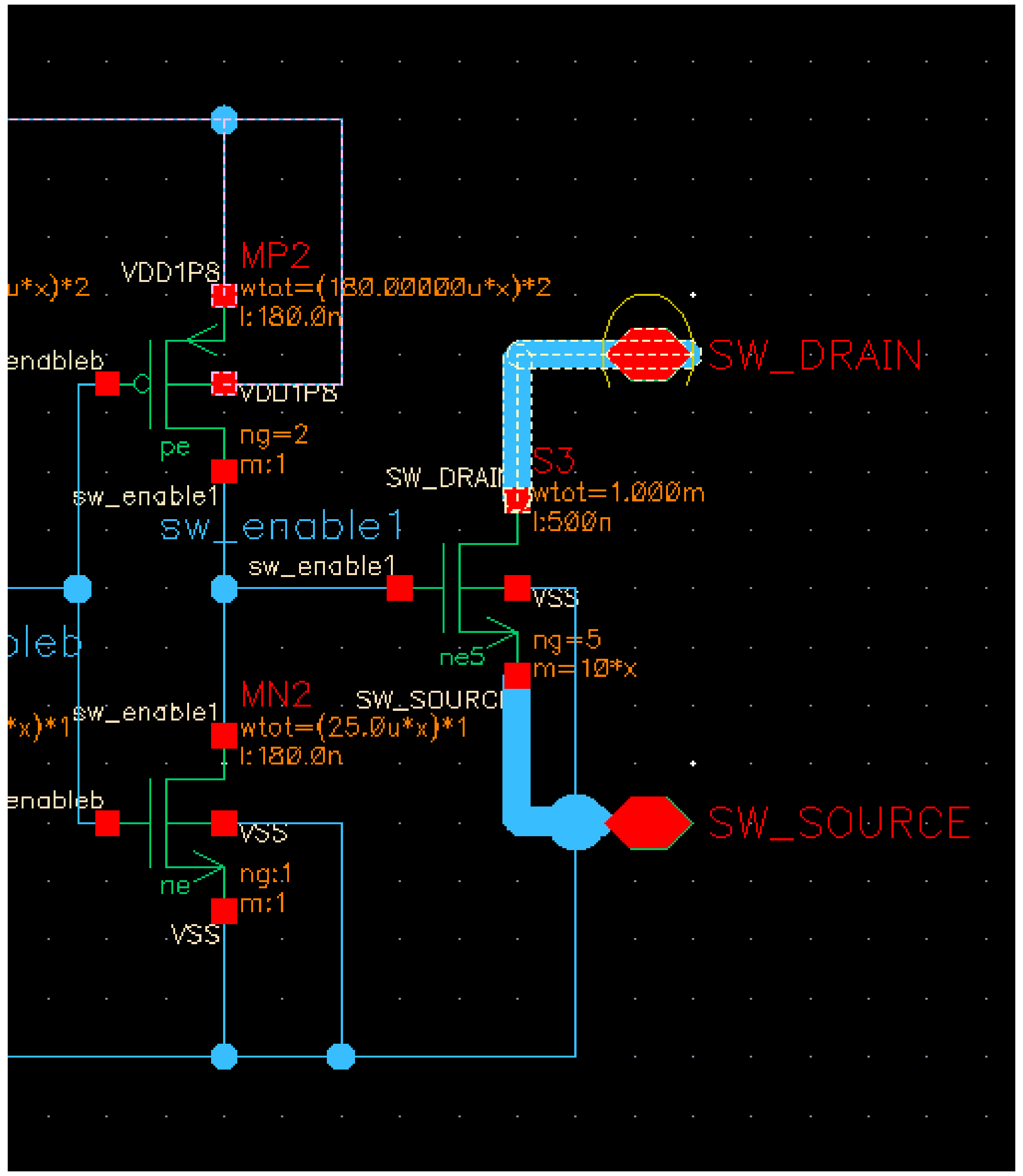
Mischief Platform IC


EN, R, AIN1[2,0], AIN2[2,0]
ael_en
Ain1
Ain2
(Vth)
100mV
Comp
SR
S
R
ael_o
R
ael_r
Reset
Dominant
Analog Event (ZC)
Detect Latch (AEL)
Edge triggered Programmable
Delays
PDS (10-1000ns)
PDM (100-1000ns)
PDL (1-1000us)
HV Rectifier
VIN_AC
QR_SN1
QR_th
ULP
Band
Gap
EN
CAL
VREF Block
8b Kelvin Varley DAC
EN
Acc
Band
Gap
Hysteretic Mode Comp
EN, B, HYST[1,0]
Ain1
Ain2
(Vth)
Comp
HYST
VIN_DC
S1_Buck
S1_Boost
COLD START
IBIAS[1,0]
EN
VDC
CS REF
(Ibias)
(Fr_Vbe)
CSO
VBIAS_OK
POR GEN
SPI CONFIG TIMING
BLOCK- PRE_ENABLES
S2
EN
VDC
Analog Cold Start
Bias Alive System
(Ancillary Boost)
(CP System)
VBIAS
(1V8)
SN1
QR_SN2
HSLT
High Speed
Low Threshold
Comp for SR
Control
L
BOOST, BUCK,
BUCK-BOOST
QR_th
VOUT
VOUT
SN2
S4
S3
GND
EN, TON CONFIG, BURST CYCLES
IC MANAGEMENT
burst
MODULATOR BLOCK
- ASYNCHRONOUS GATE DRIVES
- TON MODULATION
- 1st Valley QR Control for Buck, Boost ZVS
OUTER LOOP
CONTROLLERS
- Auto Mode Switching
- Hysteretic
- Digital State
Machines, Filters, ADC
SYSTEM
REGISTERS
IC TEST INT
SPI MASTER

- Cin=1uF+, Cout=10uF+, L=22uH
- SPI
- Power Path 0.1mm^2
- Vin_DC= 0.05 - 4V5
- Vin_AC=50V RMS (capable)
- Vout = 1V – 4V5
- 1uW – 50mW
- I_Q = 200 nW (Quiescent Power)

4-Switch Buck-Boost Converter (Non Inverting) – Design Process

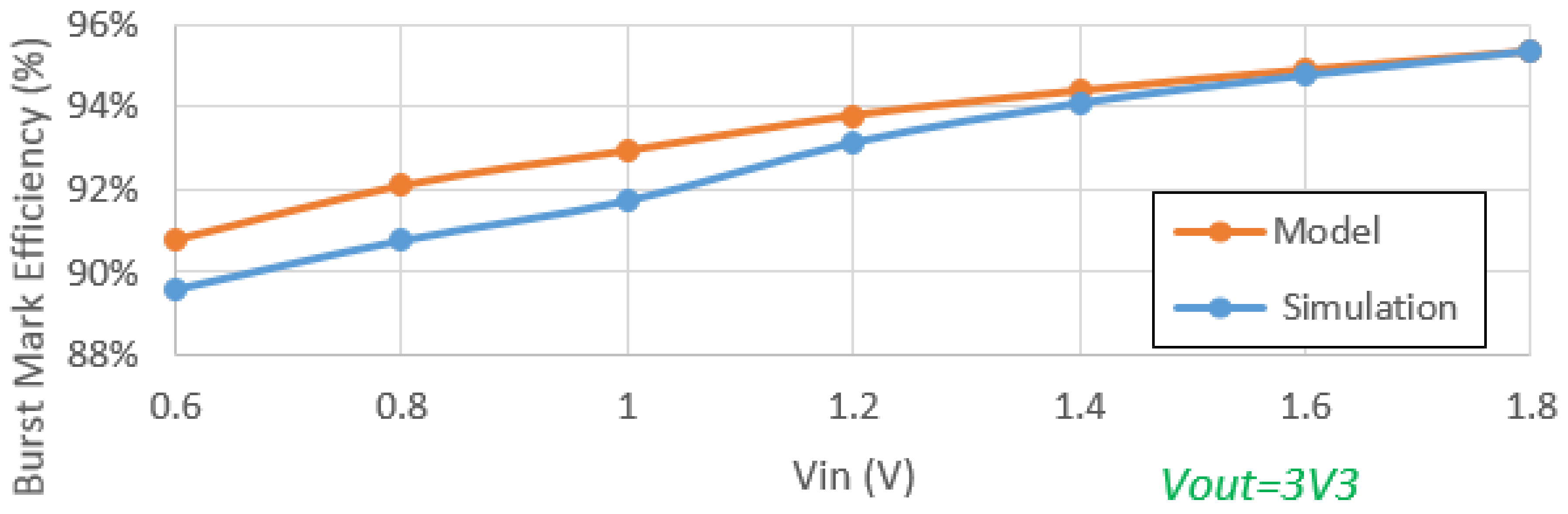
- Operating in Boost or Buck Mode – More efficient than Buck-Boost Mode
  - or time interleaved
- “Typical Application” of 1V5 to 3V3 chosen for Boost – Resonant Ring will give ZVS on S3
- Initial Switch Resistances chosen for Conduction Loss ~ 3%
- Analytical Models and Cadence used to find initial T_{ON} for maximum efficiency {1V5, 3V3, 22µH inductor}
- Cadence Parametric Sweep based ***Design Space Exploration*** by adjusting W (R_{DS_on}) for all Switches and Drivers to further increase efficiency.



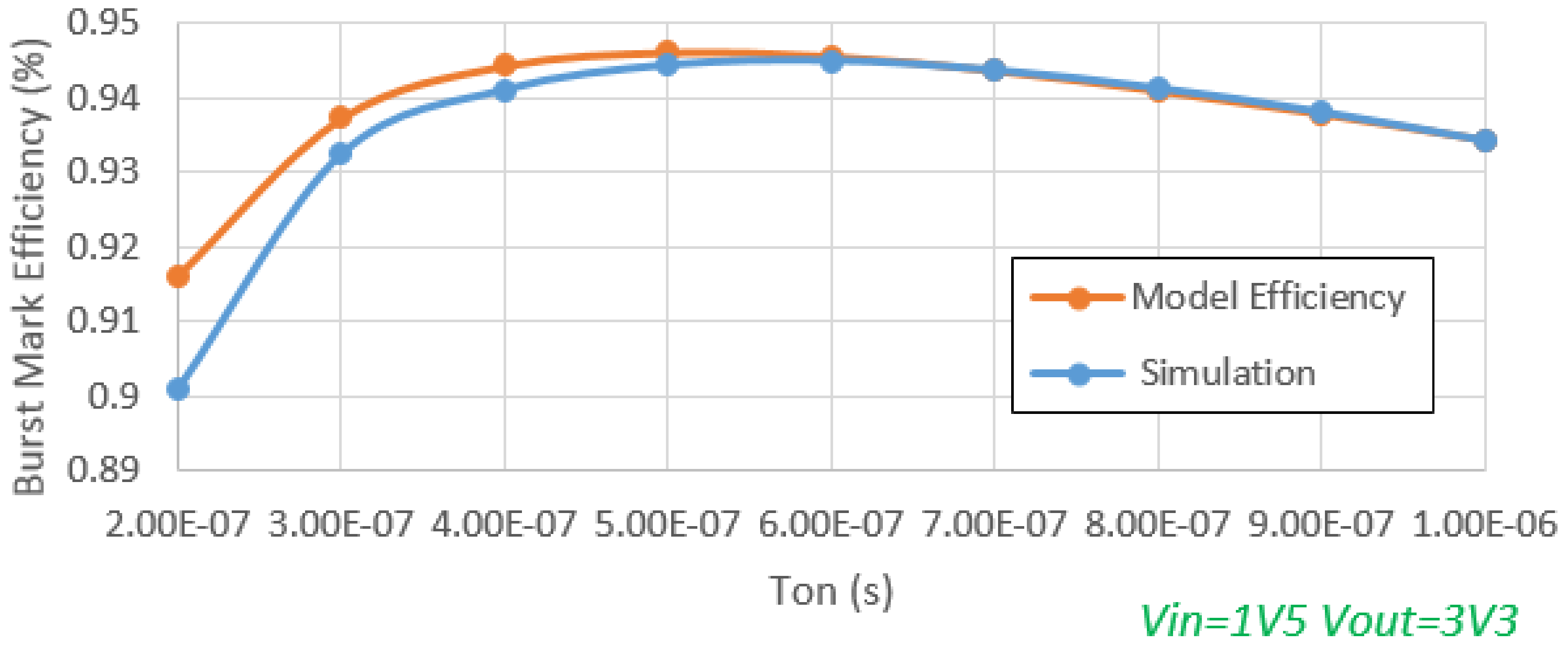
u*x)*2
VDD1P8
MP2
wtot=(180.00000u*x)*2
l:180.0n
enableb
VDD1P8
pe
ng=2
m:1
sw_enable1
sw_enable1
sw_enable1
SW_DRAIN
SW_DRAIN
S3
wtot=1.000m
l:500n
VSS
ne5
ng=5
m=10*x
leb
*x)*1
sw_enable1
MN2
wtot=(25.0u*x)*1
l:180.0n
SW_SOURCE
SW_SOURCE
enableb
VSS
ne
ng:1
m:1
VSS

MATLAB Modelling versus Cadence Top Level Simulations

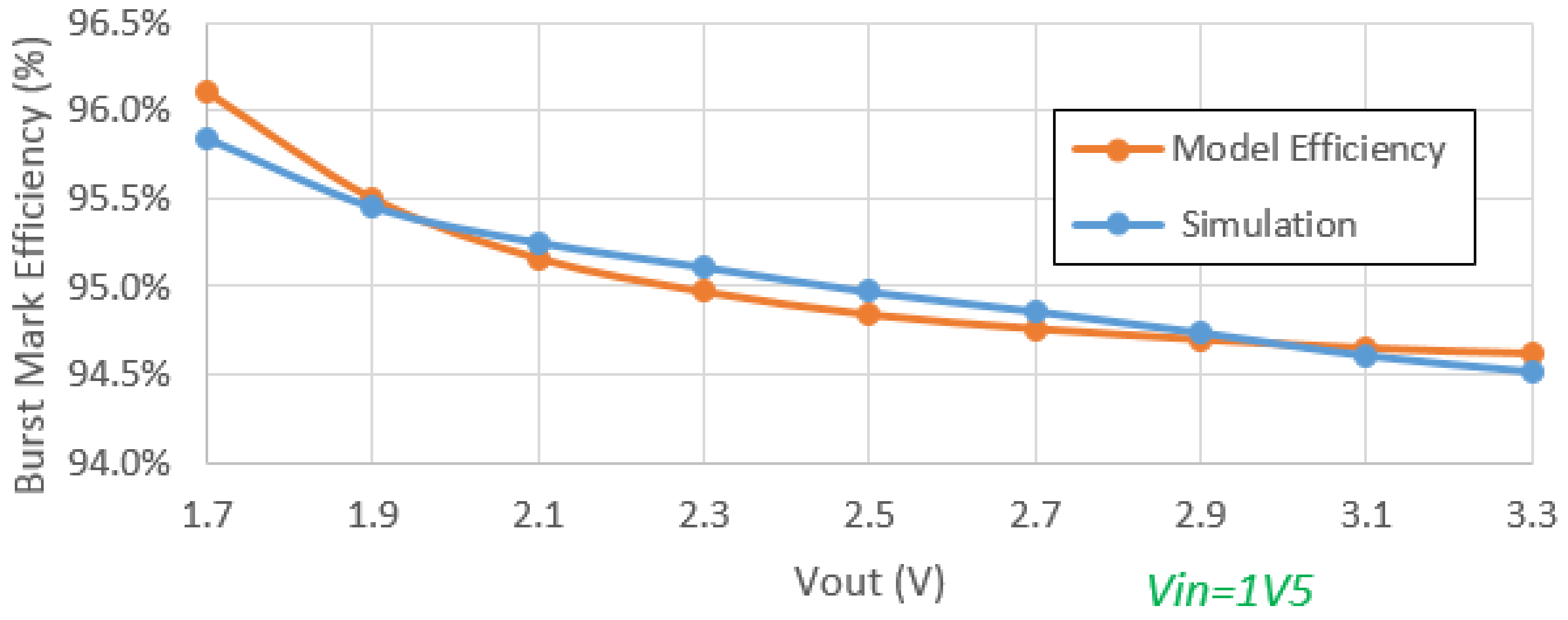
Boost Mode 4 - Model vs. Simluation (Vout=3.3)



Vout=3V3

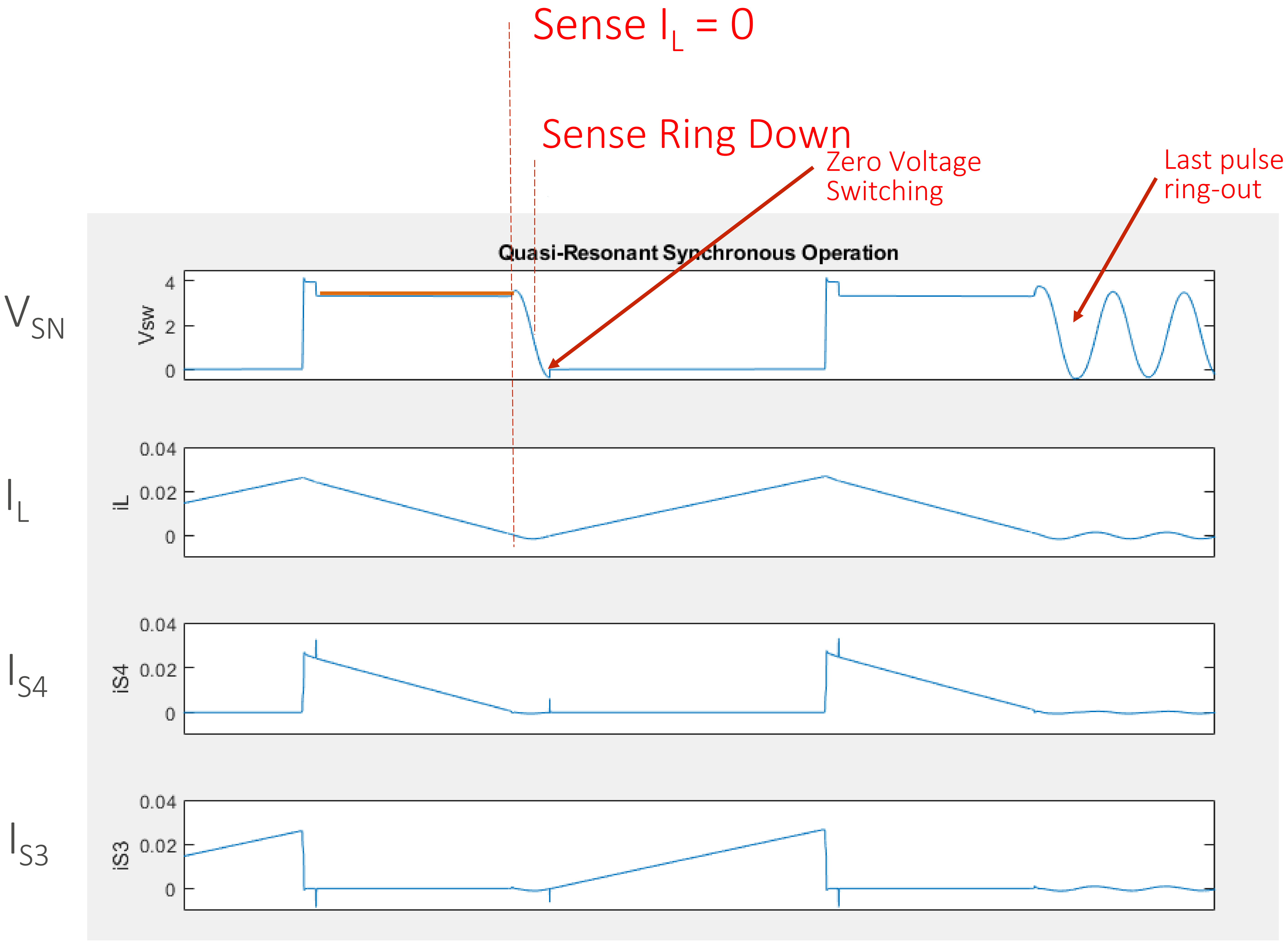


Vin=1V5 Vout=3V3



Vin=1V5

Cadence Power Path Simulations – Final 2 Pulses in Burst


Sense $I_L = 0$

Sense Ring Down

Zero Voltage Switching

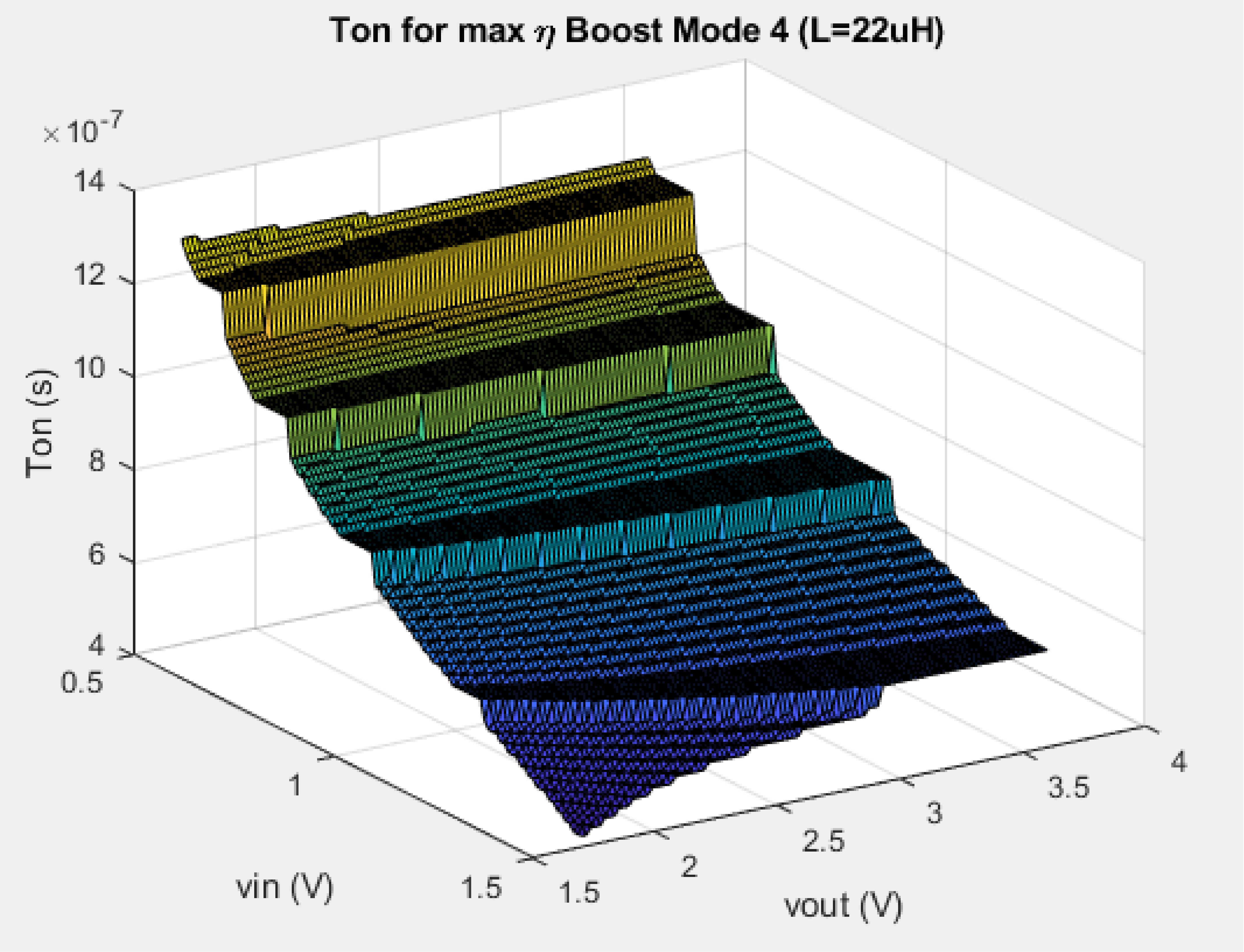
Last pulse ring-out

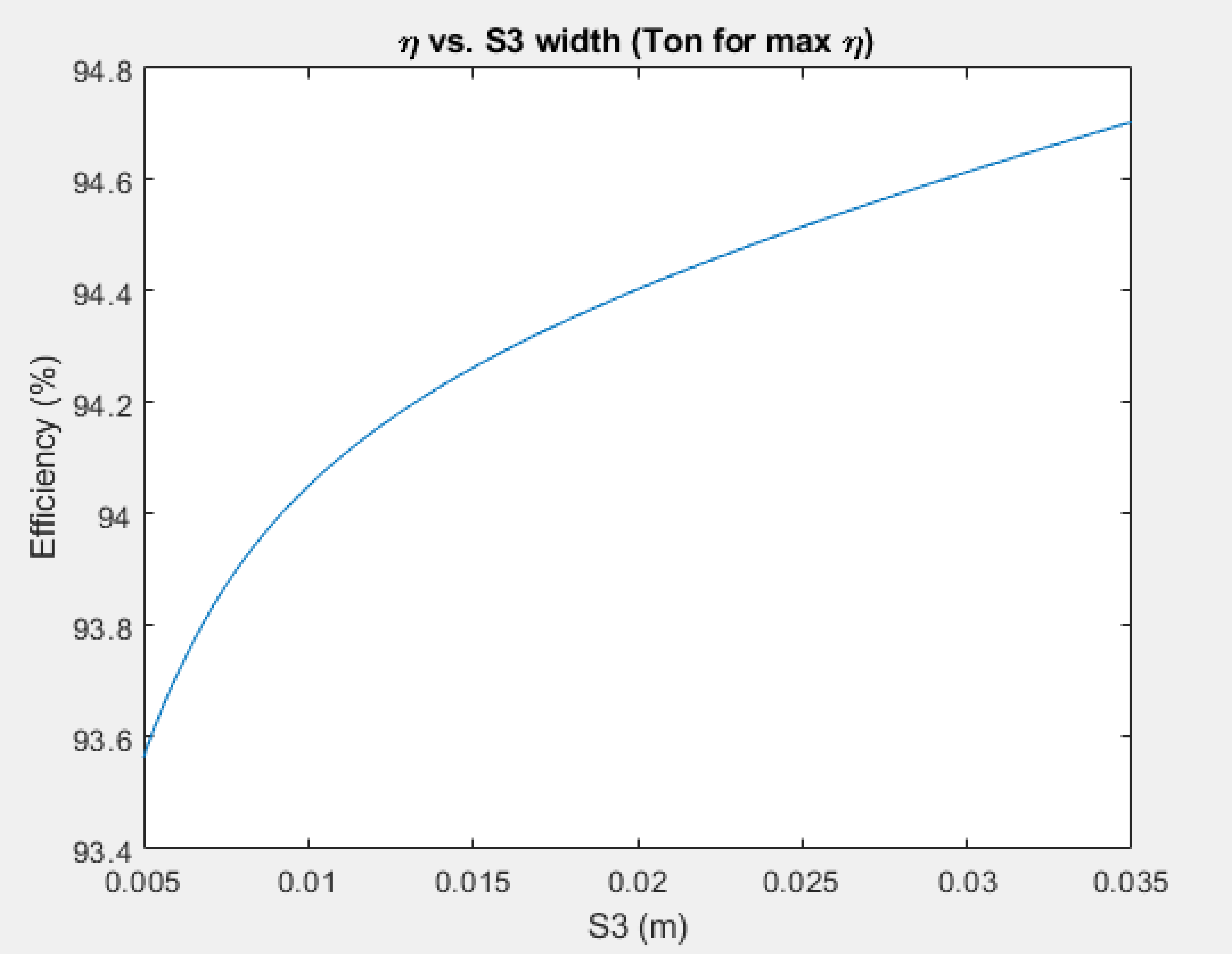
Free running

Waveforms generated by asynchronous digital state machines controlling event triggered analog latches

Design Process:

Analytically determine optimum T_{ON} Cadence Parametric Sweeps on all power path components to maximise η%

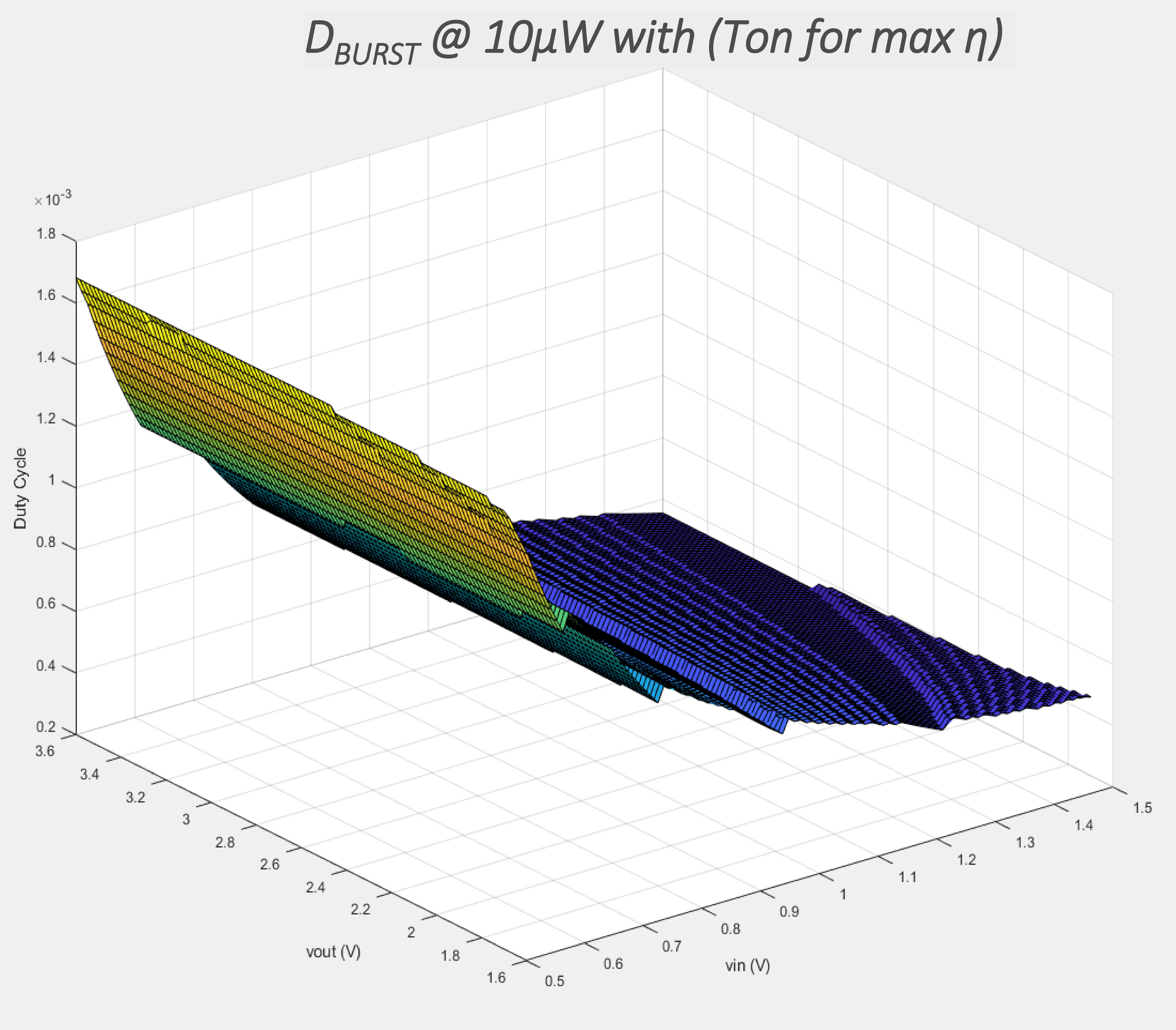




EnerHarv 2018

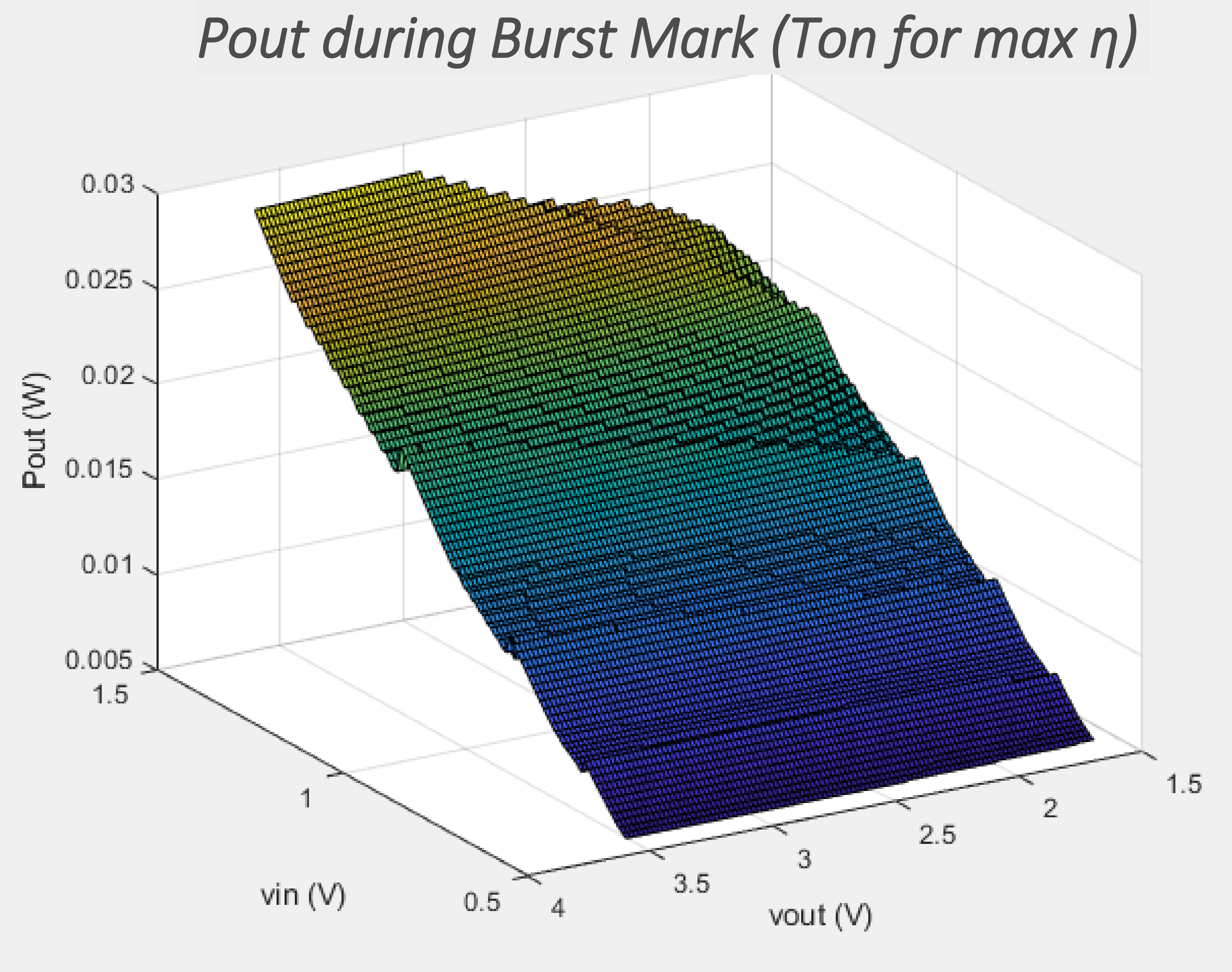
5x10^4 Dynamic Range in Pout with Ton set for maximum efficiency

Po $\propto f_{BURST}$



D_{BURST} @ 10µW with (Ton for max η)

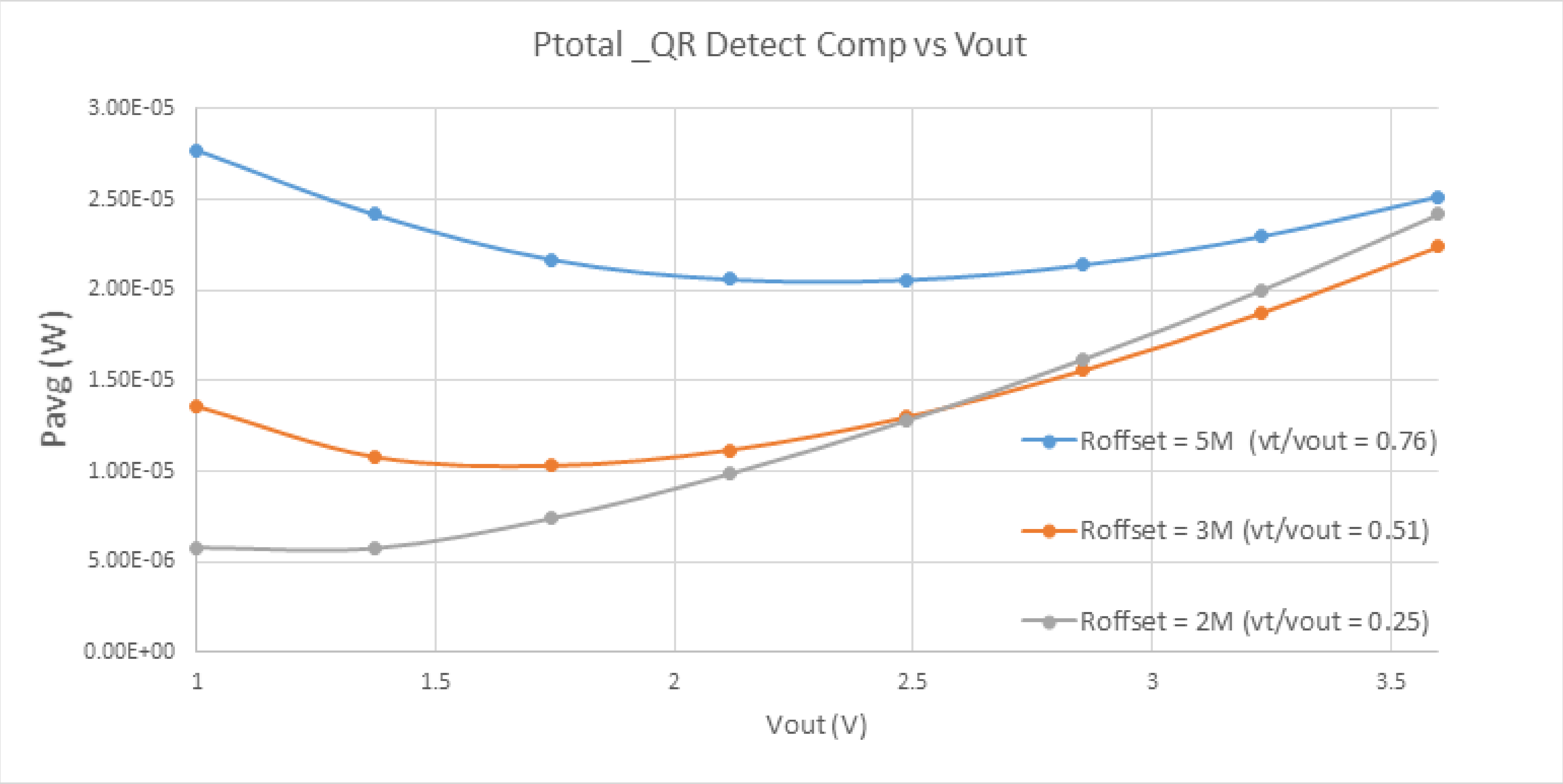
- Extend Ton or switch in parallel switches for larger dynamic range
- 10uF Cout => Vout Ripple ~0.25%
- D_{BURST} =0.0003 @ 10uW
- DCM (QR), ZCS, ZVS



Pout during Burst Mark (Ton for max η)

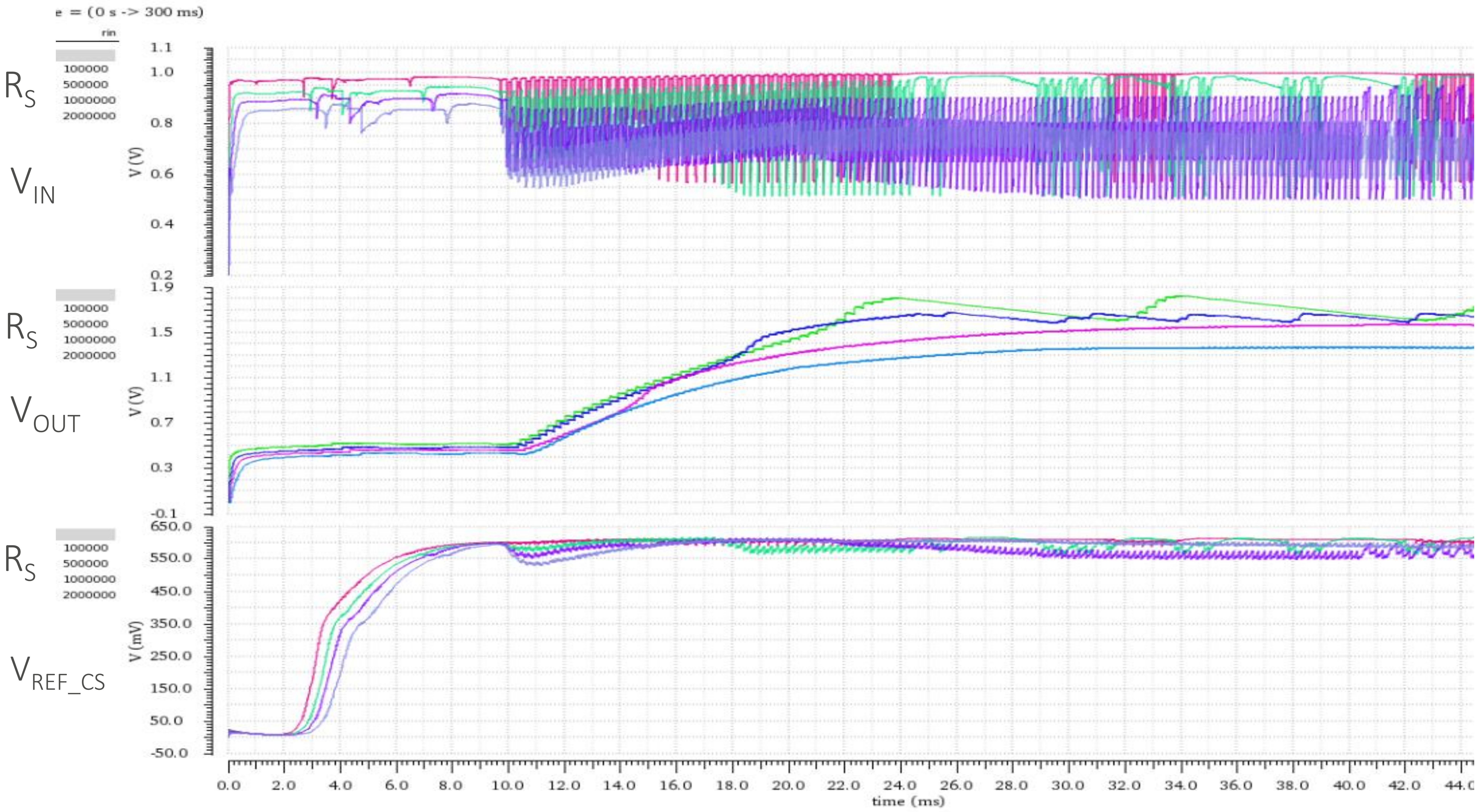
Digital Assisted Analog
Configuring: Comparator Speed and Thresholds

- Vin ~ (Vout + Vrectifier) => low di/dt => long regions passing through HSLT or QR COMP transitions
- Separating comparator thresholds by configuration gives a 3X benefit in block consumption
- Almost all low power circuits have a configurability benefit



EnerHarv 2018

Cold Start Block: Start-Up with Vin=1V, R_{SOURCE} 100kΩ – 2MΩ



2-16nA I Bias Gen

1kHz Osc

Charge Pump

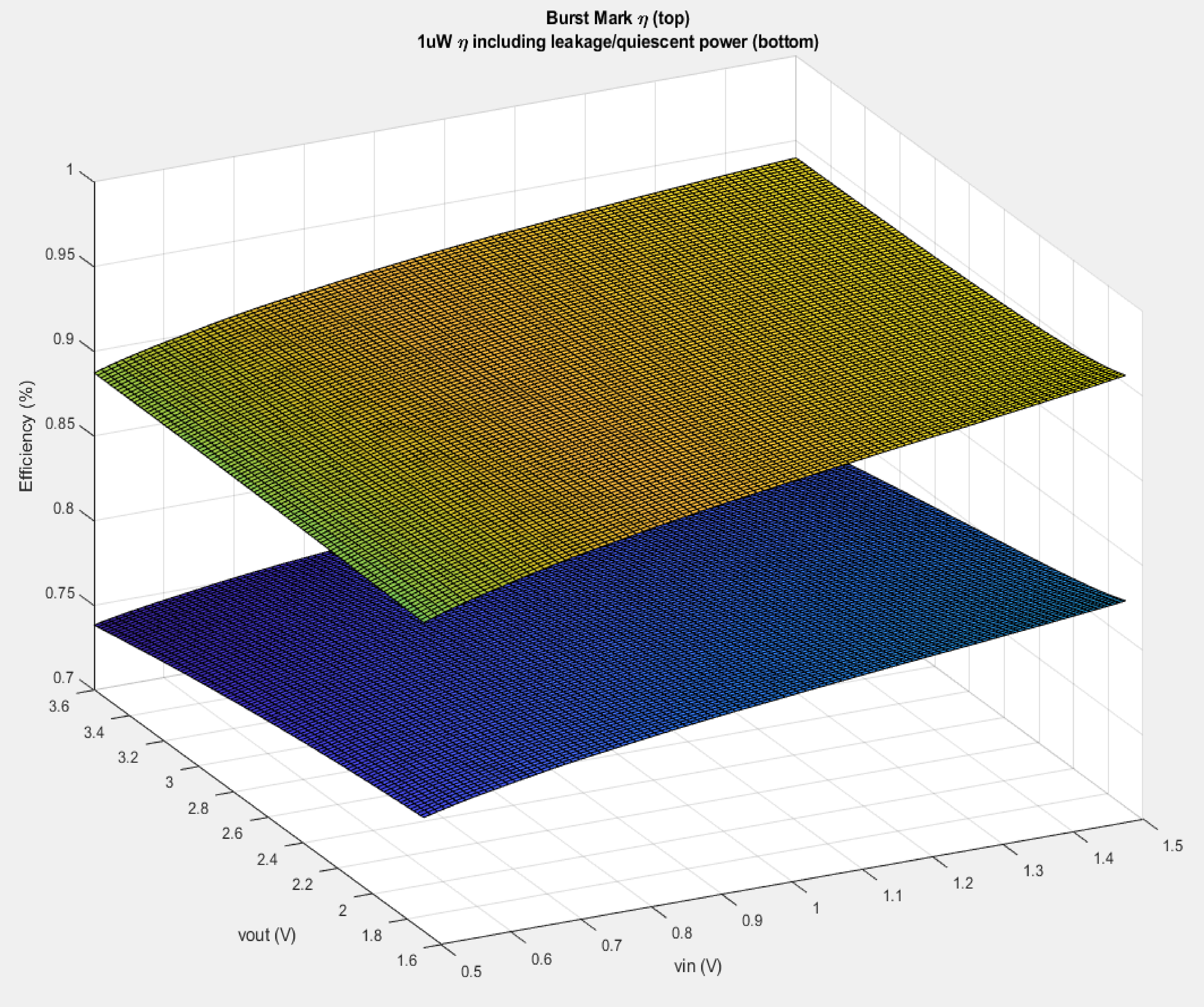
Fractional BG

DAC

Comparator

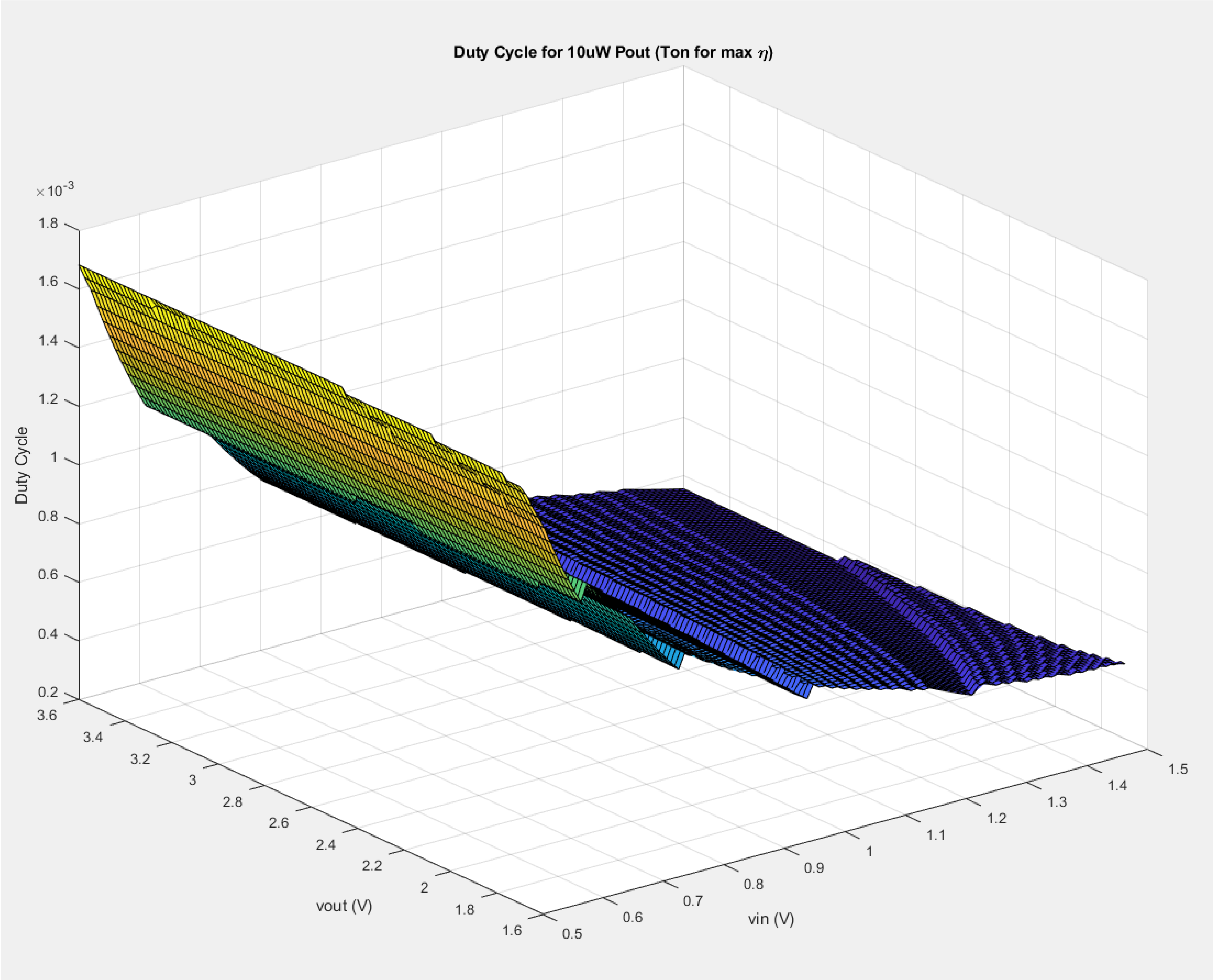
Total Current = ~60nA
V_{START} ~0.45V

Power Path Efficiency @ 1µW = 95%



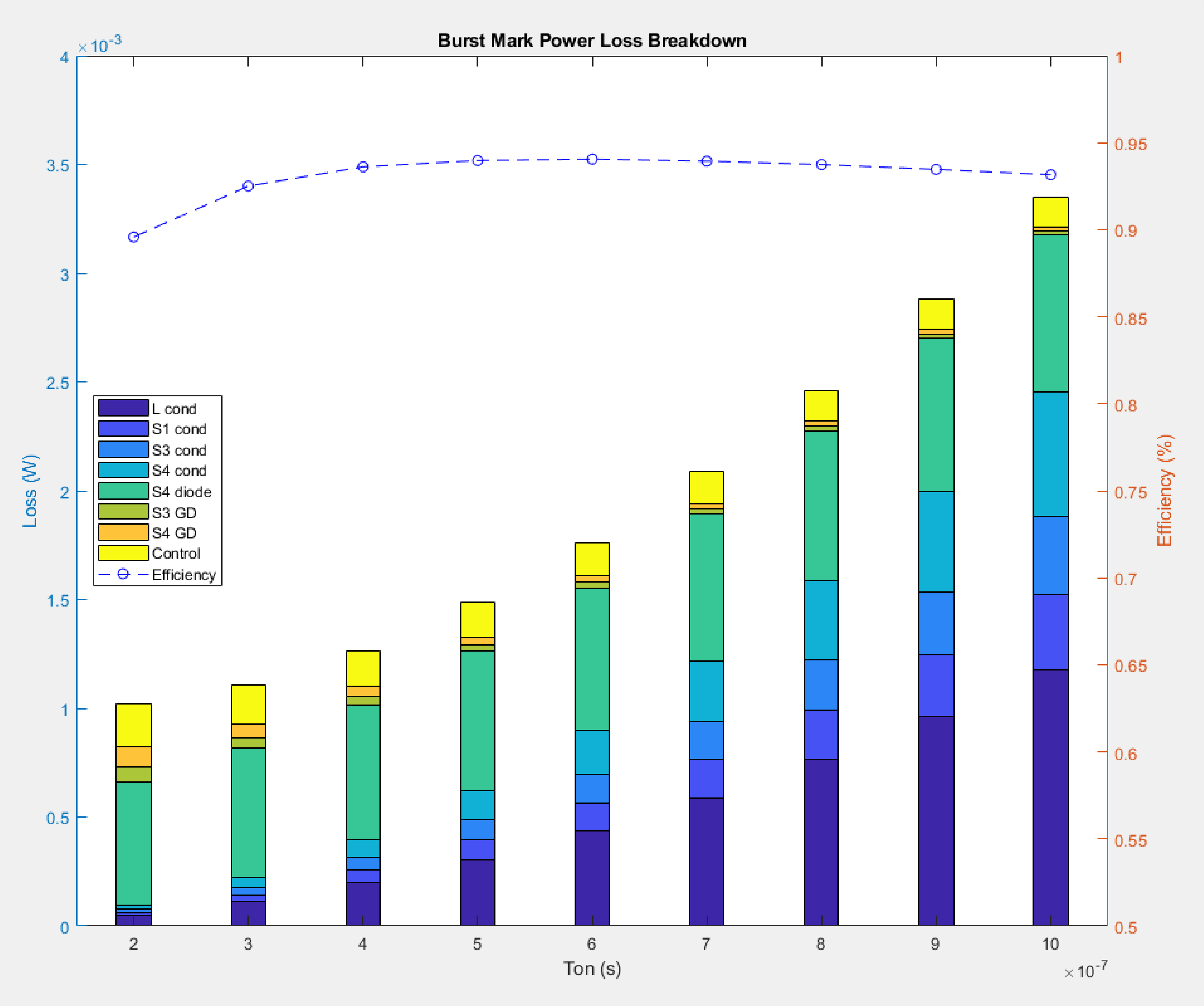
EnerHarv 2018

Burst Duty Cycle (independent of pulses per burst)



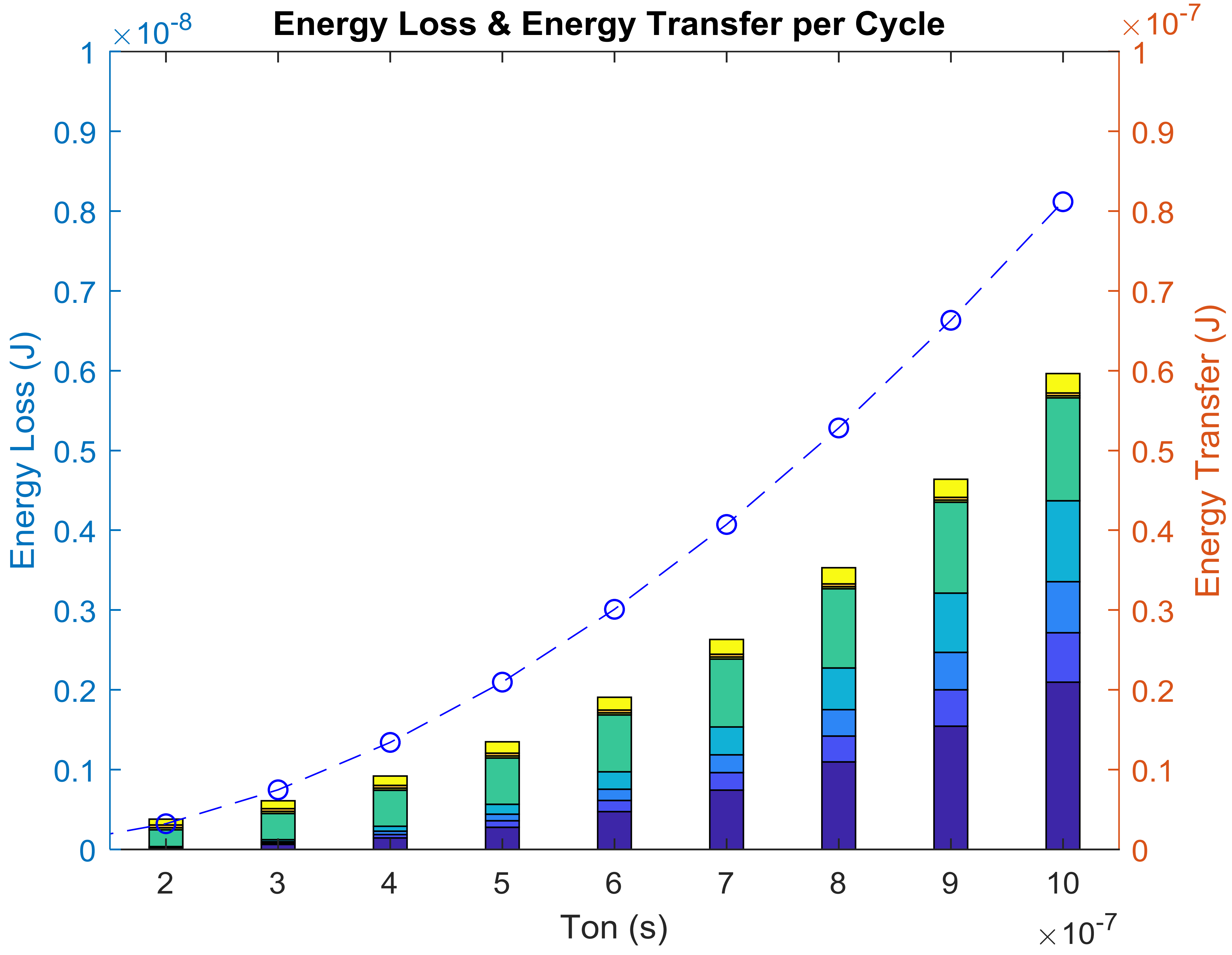
- Po = 10 uW
- D =1 in 1000

10uW, 1V5-3V3, 22uH Burst Mark Power & Efficiency vs Ton



- S1-S4 Switching Loss is very low
- S4 Body Diode Conduction could be designed out
- There is opportunity to remove the large inductor

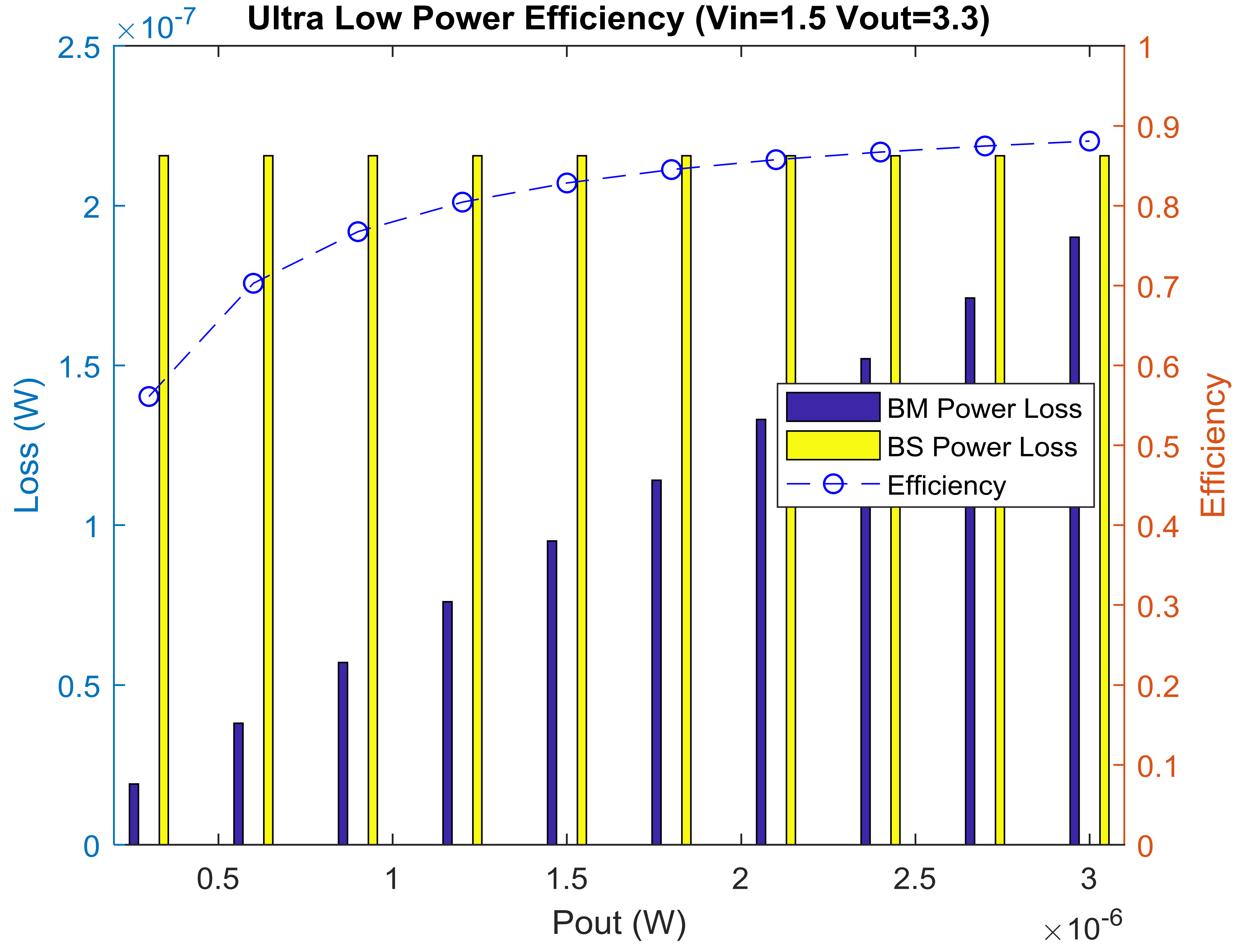
10uW, 1V5-3V3, 22uH Energy Loss and Energy Transfer per cycle vs Ton

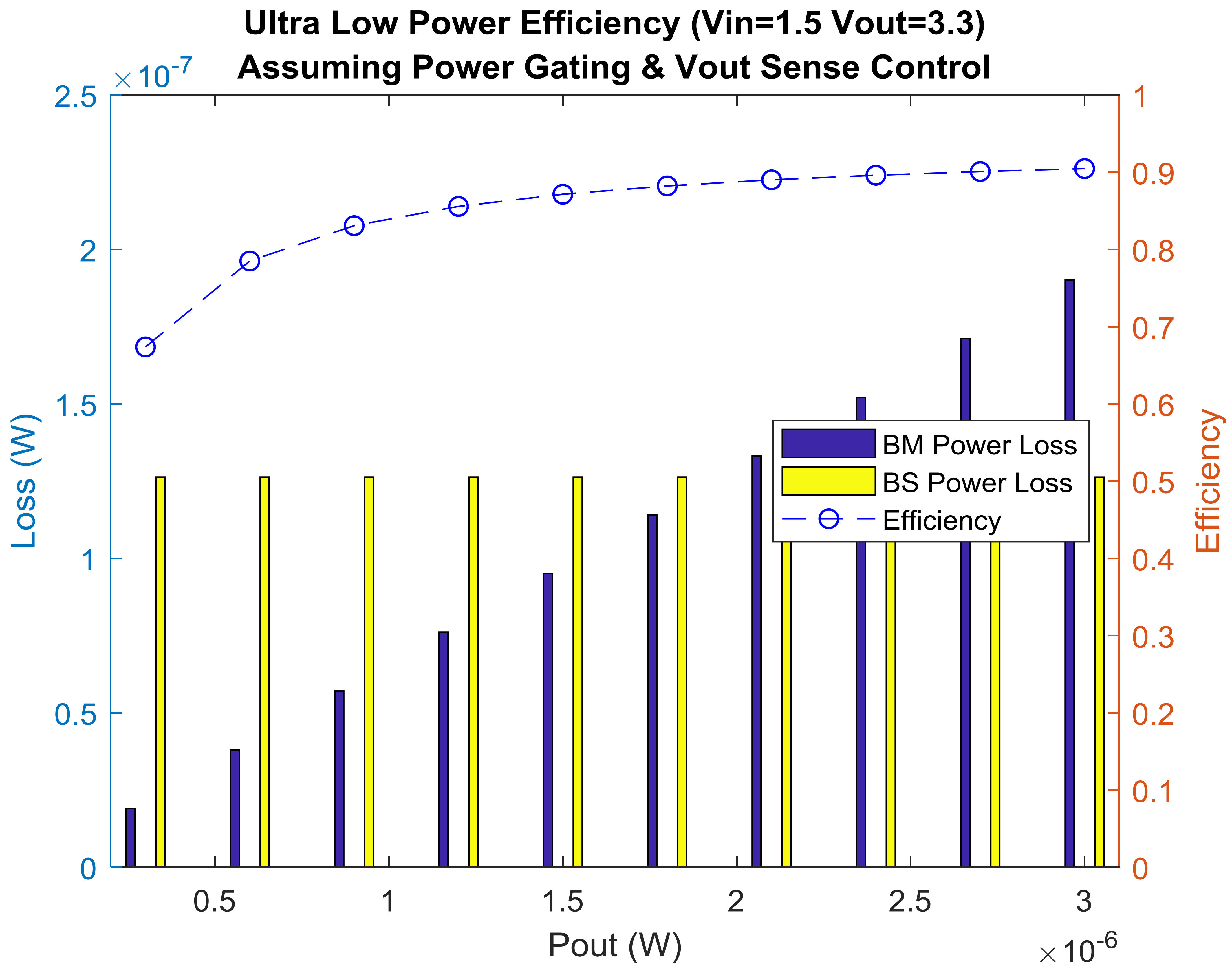


Sample IP Blocks

- 4 Switch QR Non Inverting Buck-Boost Power Path for 95% efficiency from 1uW to 10mW
- Mixed signal innovative architecture
- Extra low input voltage operation
- Asynchronous PWM Modes Generation
- Ultra efficient power path, gate drives and level shifters design
- 20nA Voltage Comparator
- 10ns Current Input Comparator
- 10ns High Side Voltage low voltage threshold Comparator
- Starved Inverter Ring Oscillators
- <100nA Cold Start: Oscillator/Charge Pump/Fractional reference system
- SPI Master Configurable Mixed Signal (external Serial EEPROM)
- High speed analog event detect latches (power cycleable)
- Variety of Digital-to-time converters (DTC)
- Ultra Low Energy ADC Systems
- Asynchronous master control state machines
- ……………

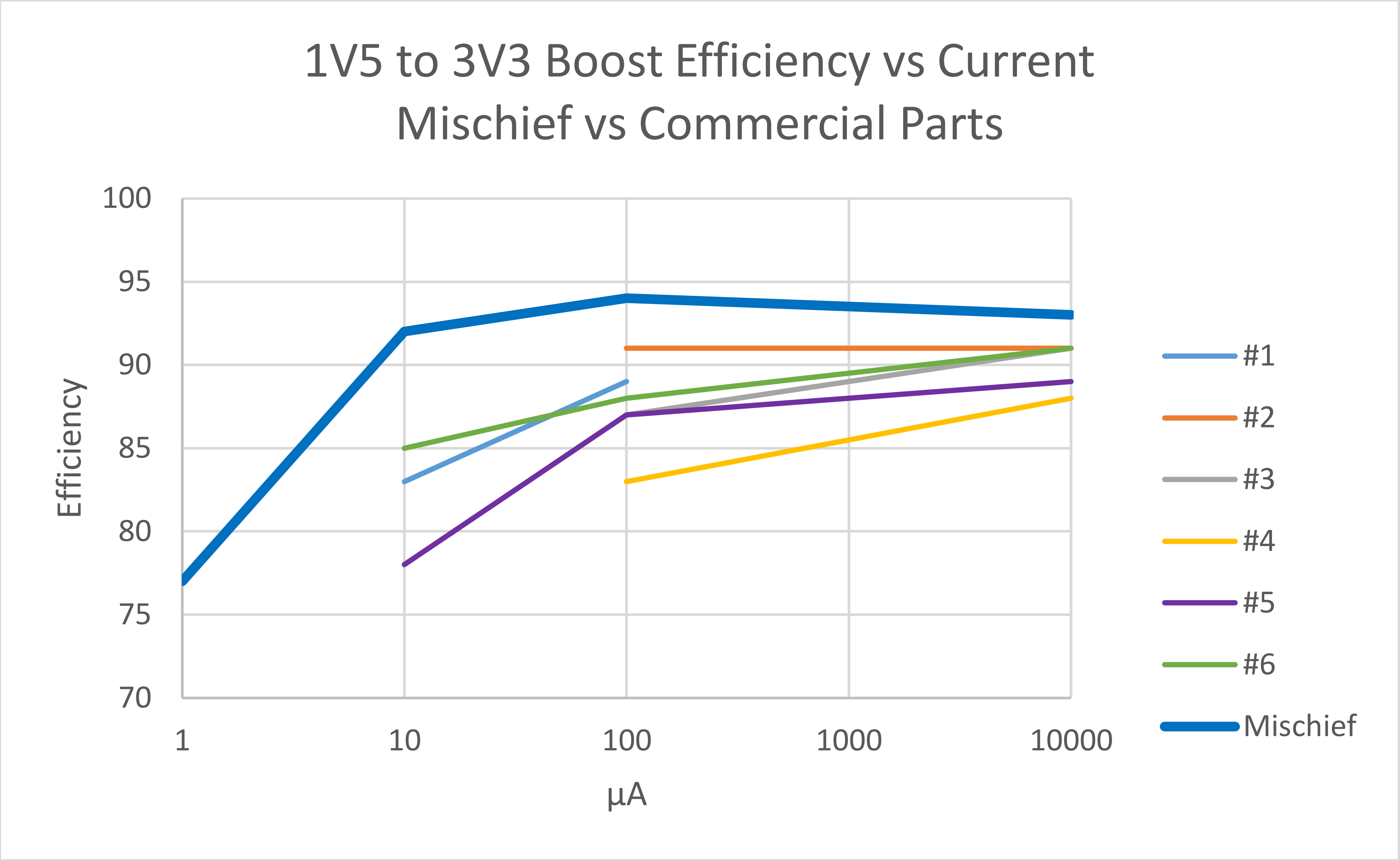
80+% efficiency @ 1µW

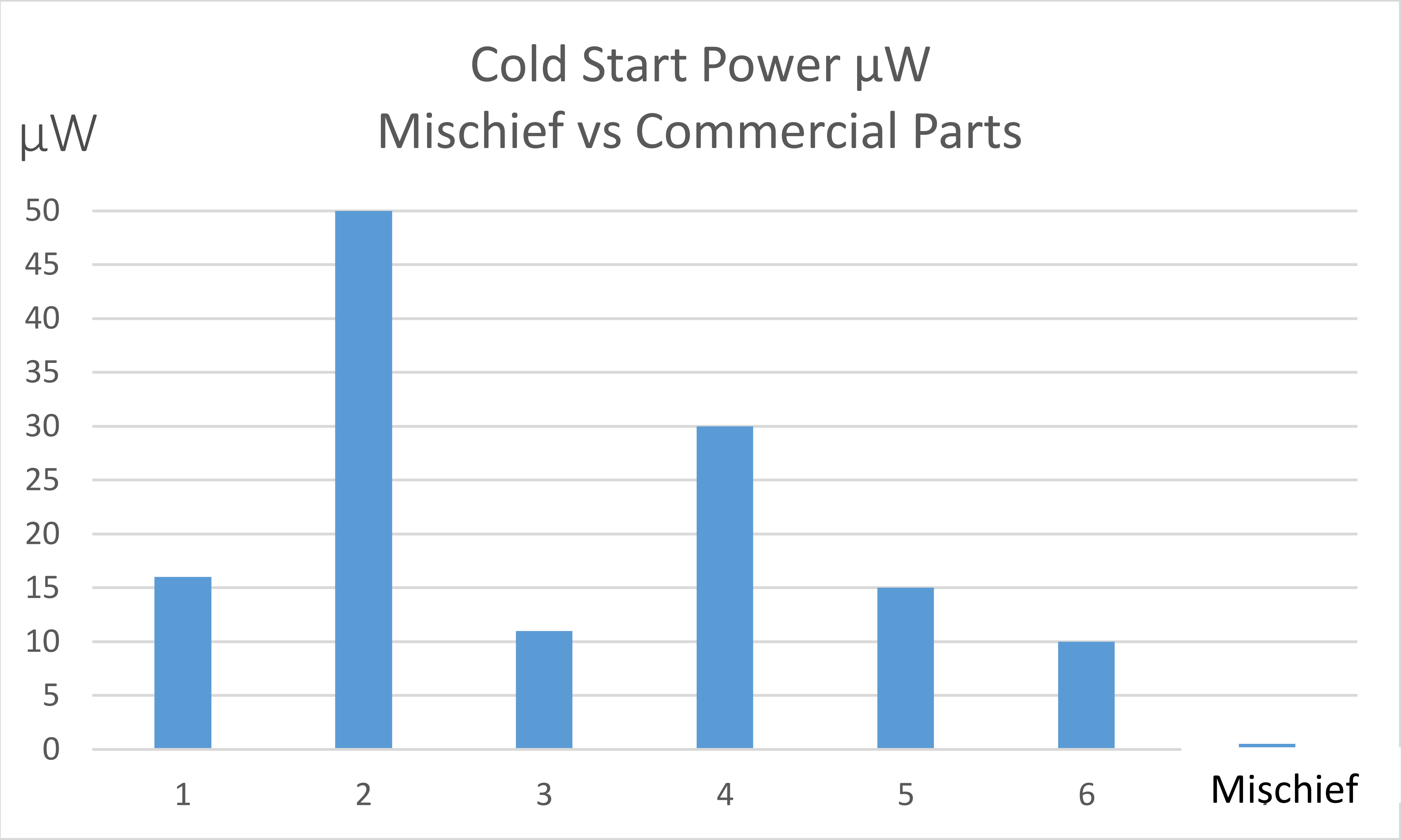




Mischief vs Commercially Available Parts (2017)

Only one part surveyed has buck-boost capability
None have advanced digital configurability (SPI)



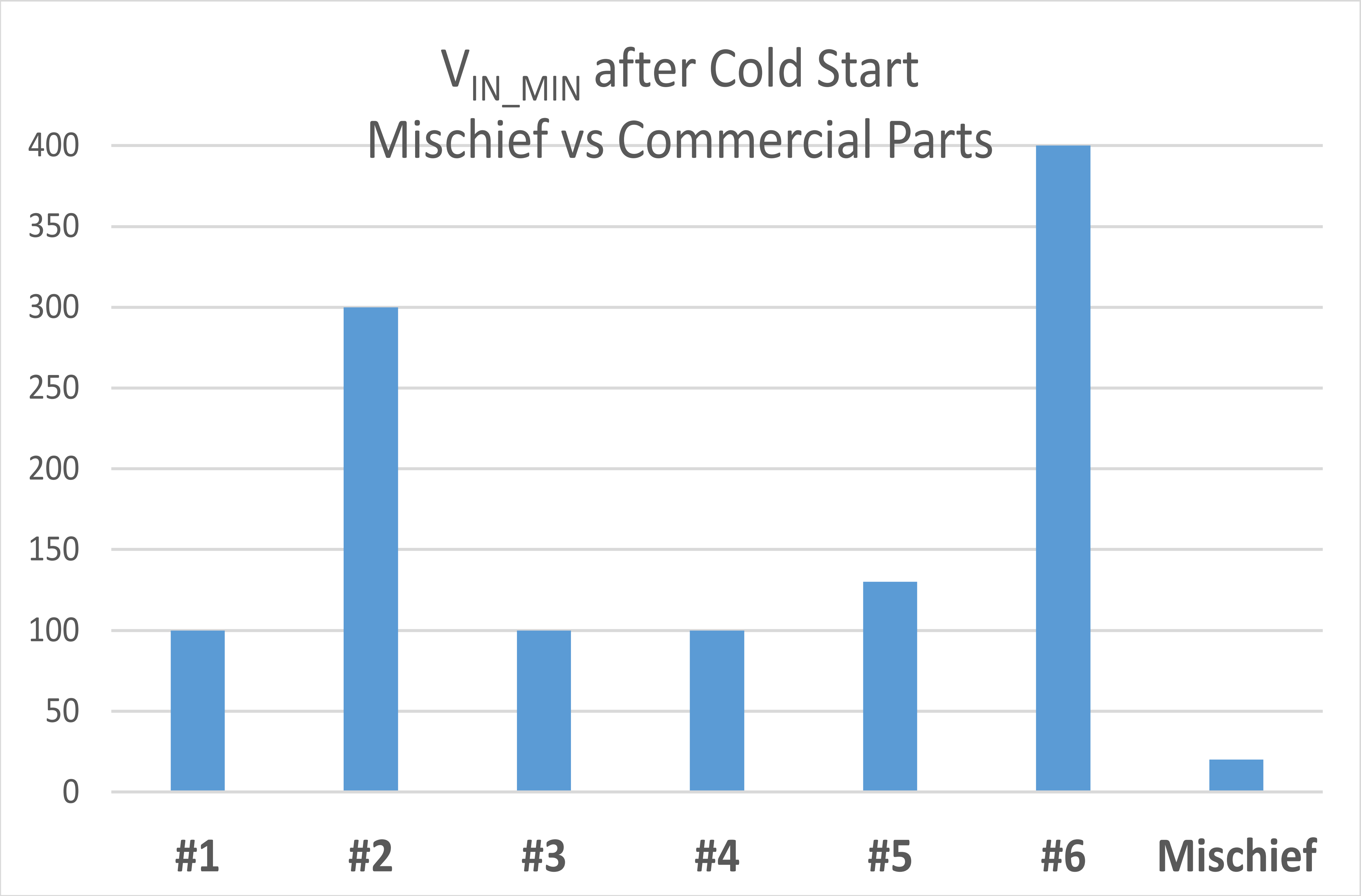


Mischief based on Top Level Schematic Sims (not LVS)

Part nos ADP5090, MB39C831, AEM10940, SPV1050, BQ25504, MAX17220

Mischief versus Commercially Available parts

Low V_{IN} operation (after Cold Start)



Marketplace EH PMIC	SPI/ I2C Interface with Host WSN Controller	Topology	Low Output Voltages
#1	No	Boost	No
#2	No	Boost	No (3V+)
#3	No	Cascade Boost, Buck+LDO	Yes
#4	No	Boost, Buck-Boost, LDO	Yes
#5	No	Boost	No (2V+)
#6	No	Boost	No
Mischief	Yes	Buck-Boost	Yes (1V+)

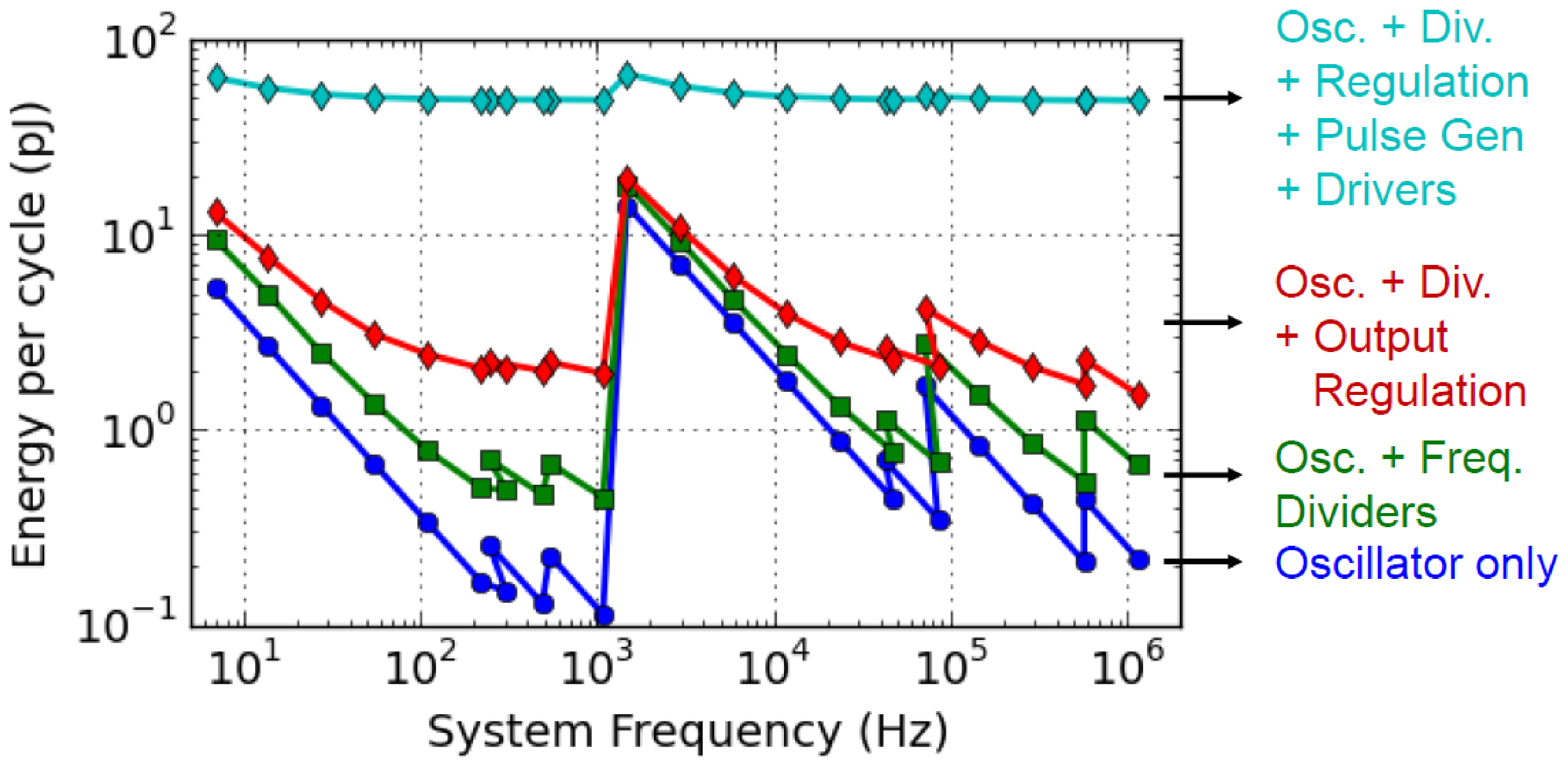
Control & Drive Efficiency vs Research

(considering 100 X Po difference between these designs)

IBM, MIT Research ISSCC'17 65nm

Overall Control Energy Loss for 240 pW Quiescent (0.8mW *max*) Buck Converter 2V-0.8V, 47uH (65nm CMOS)

V_{IN} = 2.0V, V_{OUT} = 0.8V
The energy conversion per cycle ≈1.5nJ



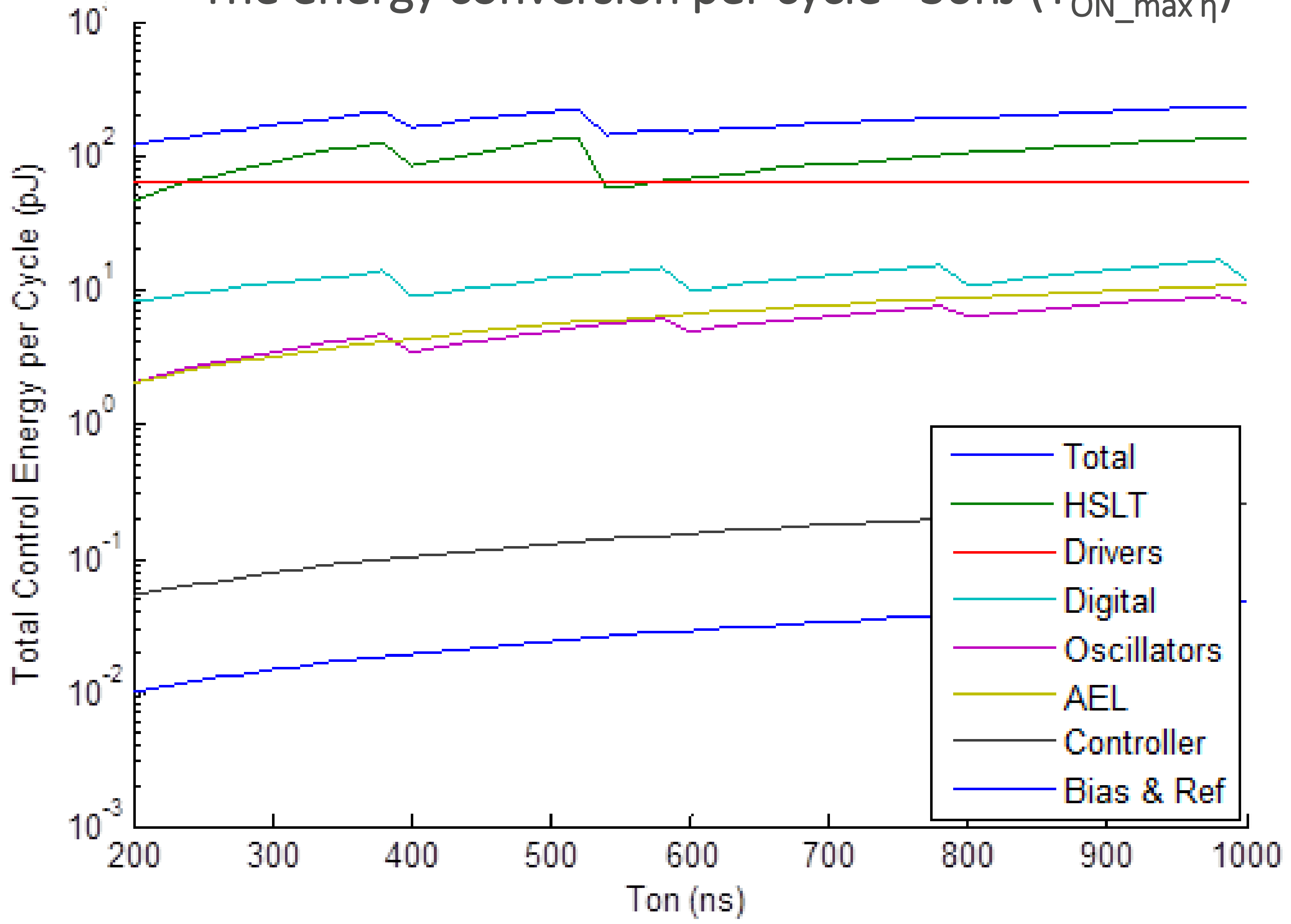
Energy Out ÷ (Control+Drive) Energy per Cycle => ($\eta_{CONTROL}$) = 95.6%

A Buck Converter with 240pW Quiescent Power, 92% Peak Efficiency and a 2x10⁶ Dynamic Range, Arun Paidimarri, Anantha P. Chandrakasan, ISSCC'17

Tyndall MCCI, Mischief '18 180nm

Overall Control Energy Loss for 200 nW Quiescent (27mW @$T_{ON\_max\ \eta}$) Buck-Boost Converter 1V5-3V3, 22uH (180nm CMOS)

V_{IN} =1.5V, V_{OUT} =3.3V
The energy conversion per cycle ~30nJ ($T_{ON\_max\ \eta}$)



Energy Out ÷ (Control+Drive) Energy per Cycle => ($\eta_{CONTROL}$) = 98.83% (@ $T_{ON\_max\ \eta}$ = 600ns (max. η)

S3_GD =27pJ, S4_GD=34pJ @ Ton = 600ns for 1V5 to 3V3, 1kHz/1ms Burst Space assumed = 200pJ

Conclusions

Advanced real time system optimisation is feasible for highly featured 350nW+ designs

Advanced digital modulators and control are applicable, next step - add ULE ADC
Digital filtering and outer loops may be implemented by node host controller

Power System Design selects T_{ON} for maximum efficiency at all points – Host -> SPI -> Config Benefit

Extensive Matlab modelling and top level Cadence simulation match-up

Our Control and Modulator Energy Efficiency is very high

Our Quiescent Current could be substantially reduced by HSLT redesign, switched senses and power gating

Our architecture is future proofed for considerably higher frequencies

Our architecture is applicable for maximising energy transduction and efficiency for a wide range of emerging MEMs and Micro Scale Systems

IP for IoT Node ASICs, SoCs

Team

- James McCarthy
- Tim Daly
- Gerry McGlinchey

- Ivan O’Connell, Séamus O’Driscoll

Thank You

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