Methodologies for Reducing ULP Device Power Consumption

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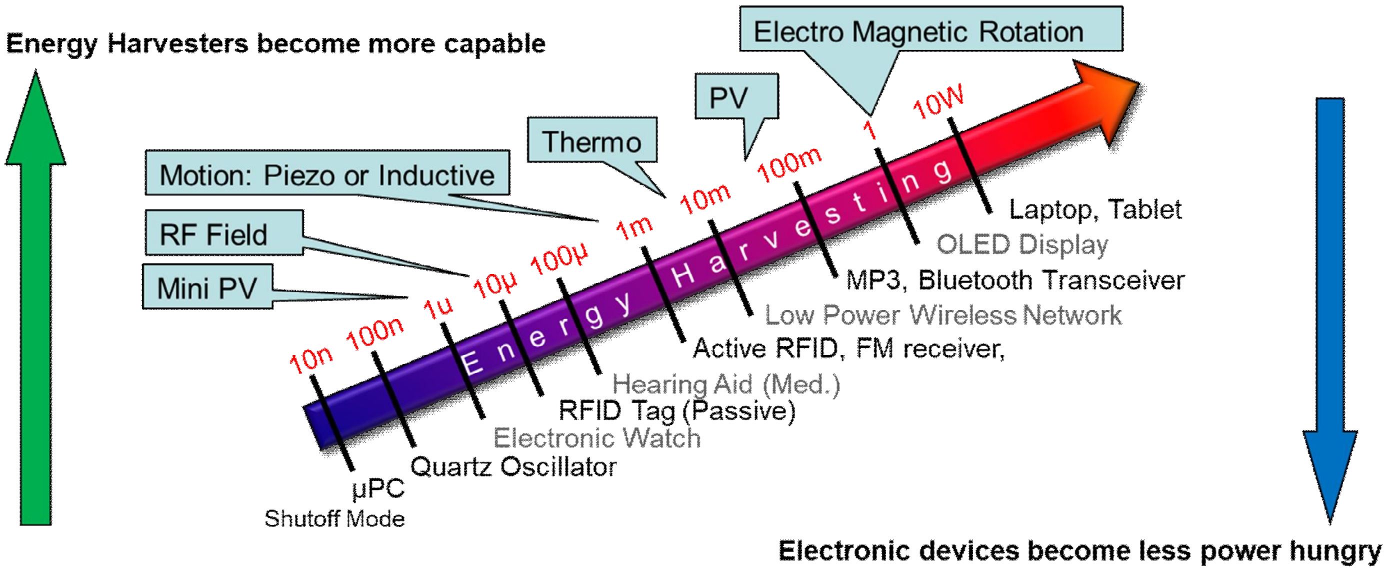
Energy Harvesting

- **Typical energy harvester output power**

RF:	0.1μW/cm²	0.01mV
Vibration:	1mW/cm²	0.1 ~ 0.4 V
Thermal:	10mW/cm²	0.02 ~ 1.0 V
Photovoltaic:	100mW/cm²	0.5 ~ 0.7 V typ./cell



Source: *Lorandt Foelkel, "Energy Harvesting Seminar," Wurth Elektronik eiSos, 2013*

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Motivation

- Address the “Energy Gap”
- Designers always look for ways to reduce unwanted components of power consumption
  - architecting the design in a fashion which includes low power techniques
  - adopting a process which can reduce the consumption
- Always done at the expense of performance, reliability, chip area, or several of these
  - one has to reach a compromise between power, performance, and cost

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Ultra Low Power Drivers

- Battery Powered Systems – Phones
  - Mobile revolution has really driven need for low power design
- High-Performance Systems – Server Farms
  - Cost of removing the unused energy → Heat
  - Reliability
- IoT
  - Deploy and forget devices
  - Cost of transmitting data → move processing being done at the edge

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How to achieve this?

- Dynamic Power Consumption
- Static Power Consumption
- Process Technology
- Architectural decisions

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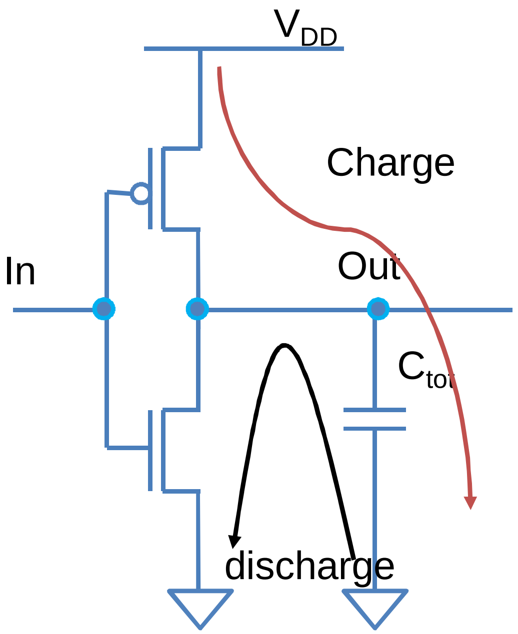
Dynamic Power Consumption

- Switching & short circuit power
- $P_{dyn} = \alpha C_{tot} V_{DD}^2 F$
  - $C_{tot} = C_{load} + C_{par}$
  - V_{DD} - Supply Voltage
  - F – clock Frequency



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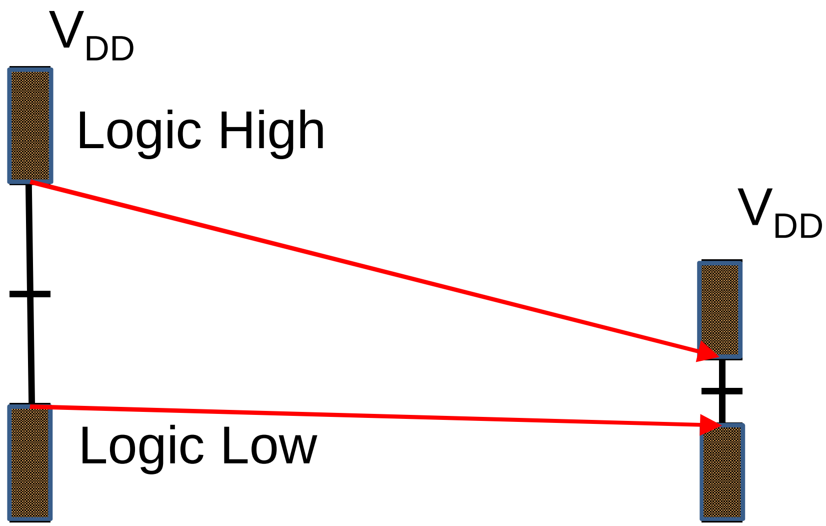
Voltage Scaling – Reducing the Supply Voltage



Limited by the ability to accurately differentiate between a 1 and 0

Clock Gating

- Remove unnecessary switching activity
- Only clock necessary blocks
- Remove clock from other blocks

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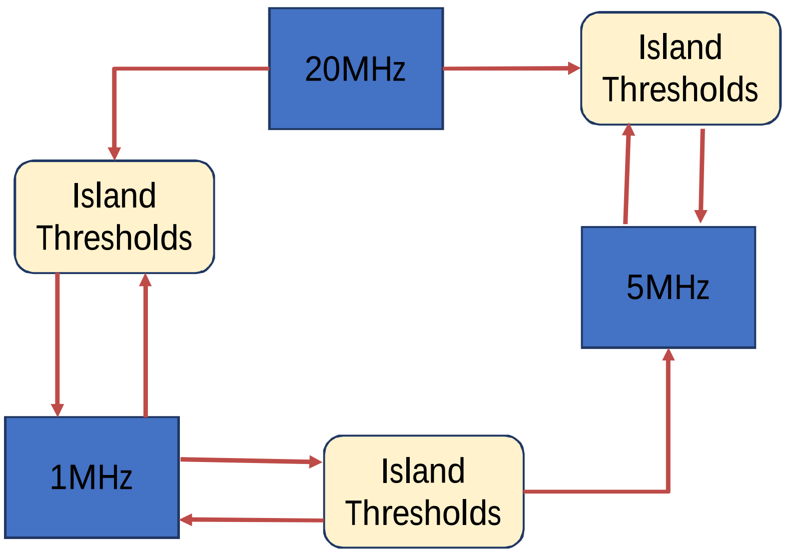
Frequency scaling

- Clock frequency adjusted to meet requirements
- Frequency islands



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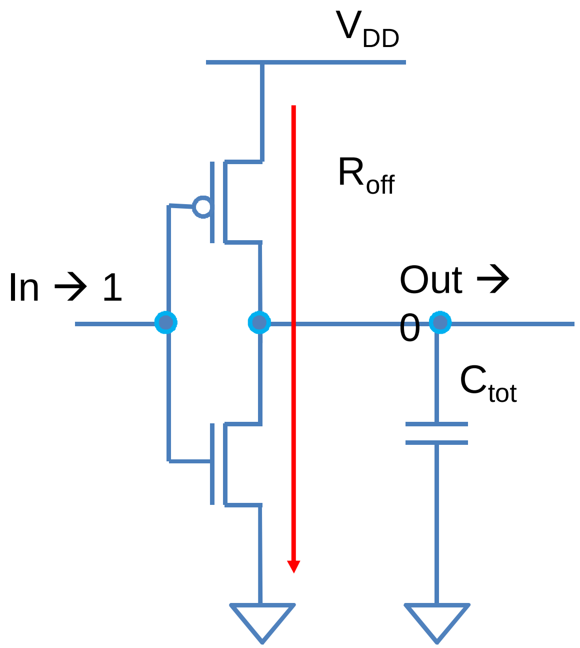
Asynchronous logic

- Synchronous
- Clock Driven
- P_{dyn} → activity independent

- Asynchronous
- Event Driven
- P_{dyn} → activity dependent

Static – Leakage Power Reduction

- The power a circuit consumes when it's doing nothing!
- Finite off Resistance
- $P = k\,V_{DD}$
  - Voltage scaling
  - Technology
  - Device Selection
    - High Vt Devices



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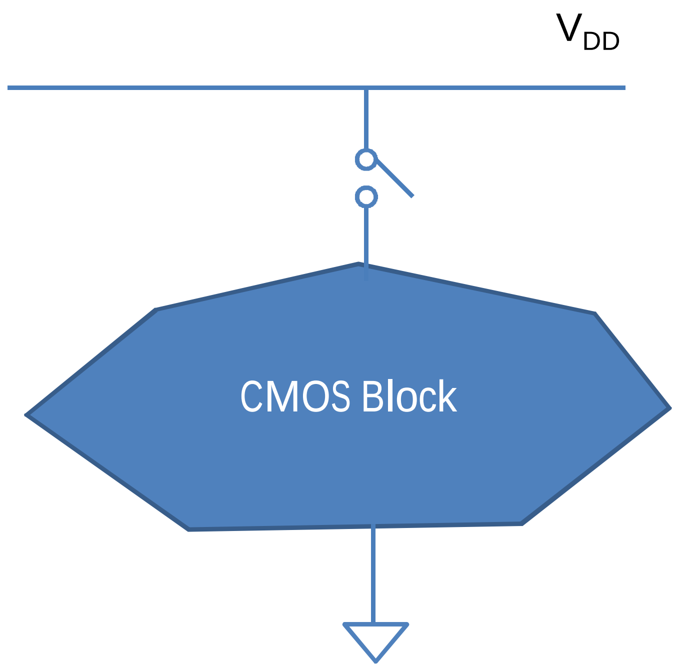
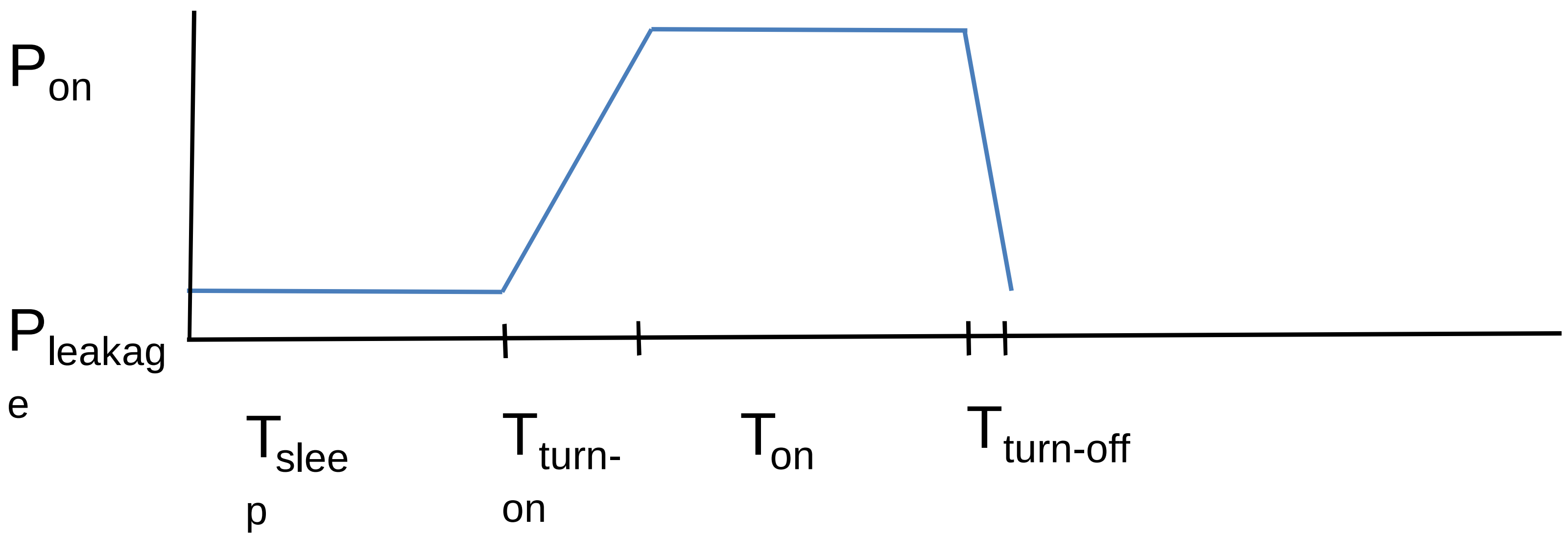
Power Gating

- Remove the power to inactive blocks
- Leakage Power → zero



Power Duty Cycling

- Turning on and off sub-blocks to mininise the power consumption



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Power Duty Cycling

- t_{sleep} – time the device spends in sleep mode
- $T_{turn\text{-}on}$ – time the device/block takes to turn on
- T_{on} – active time
- $T_{turn\text{-}off}$ – time it takes to turn the device/block off

- Objective
  - $P_{avg} = 2x\ P_{leakage}$
    - e.g. $P_{on} = 100X\ P_{leakage}$
    - $T_{sleep} = 100\ X\ T_{on}$

Limited by the Leakage Current

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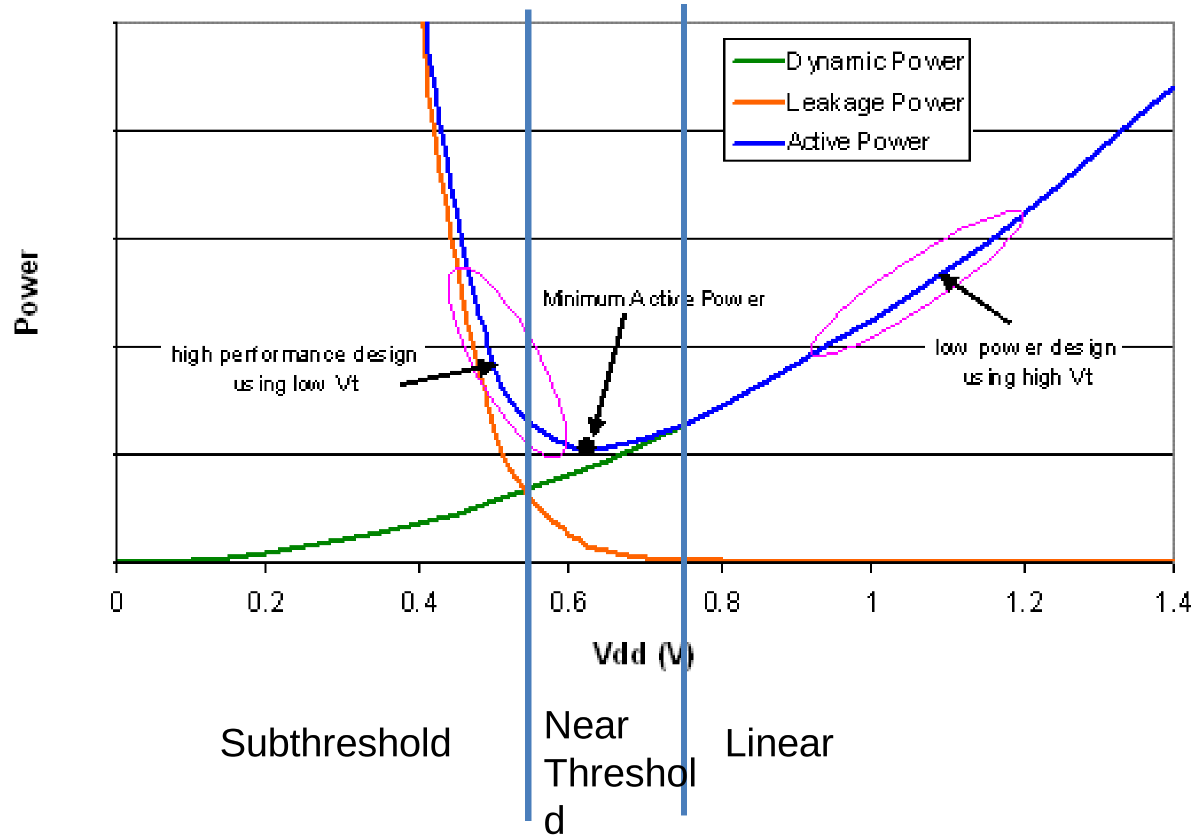
MOS Transistor Regions of operation

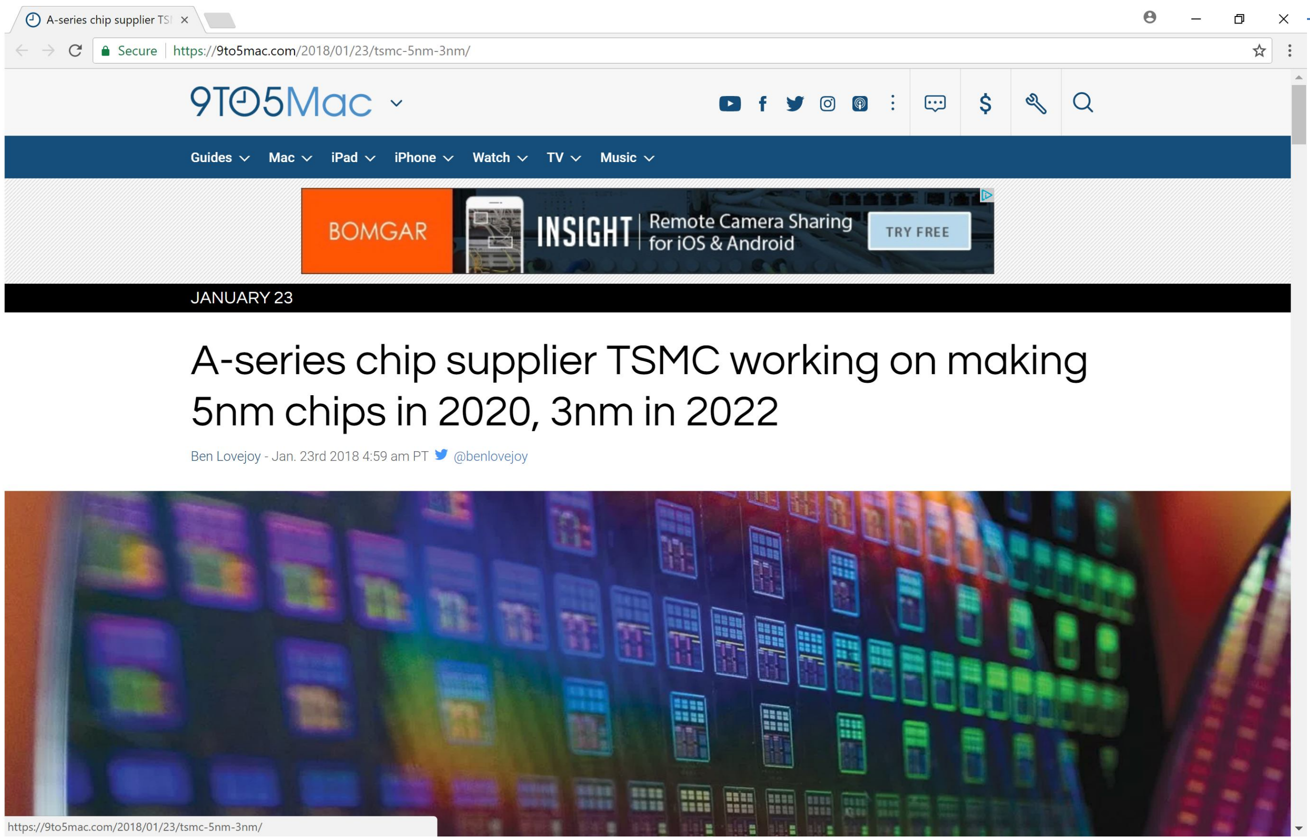
- Linear Region
- Near Threshold
- Sub Threshold

Active Power vs Vdd at Constant Frequency



Source: www.design-reuse.com/news_img/20090316b_5.gif

Technology Scaling – Moore – More than Moore



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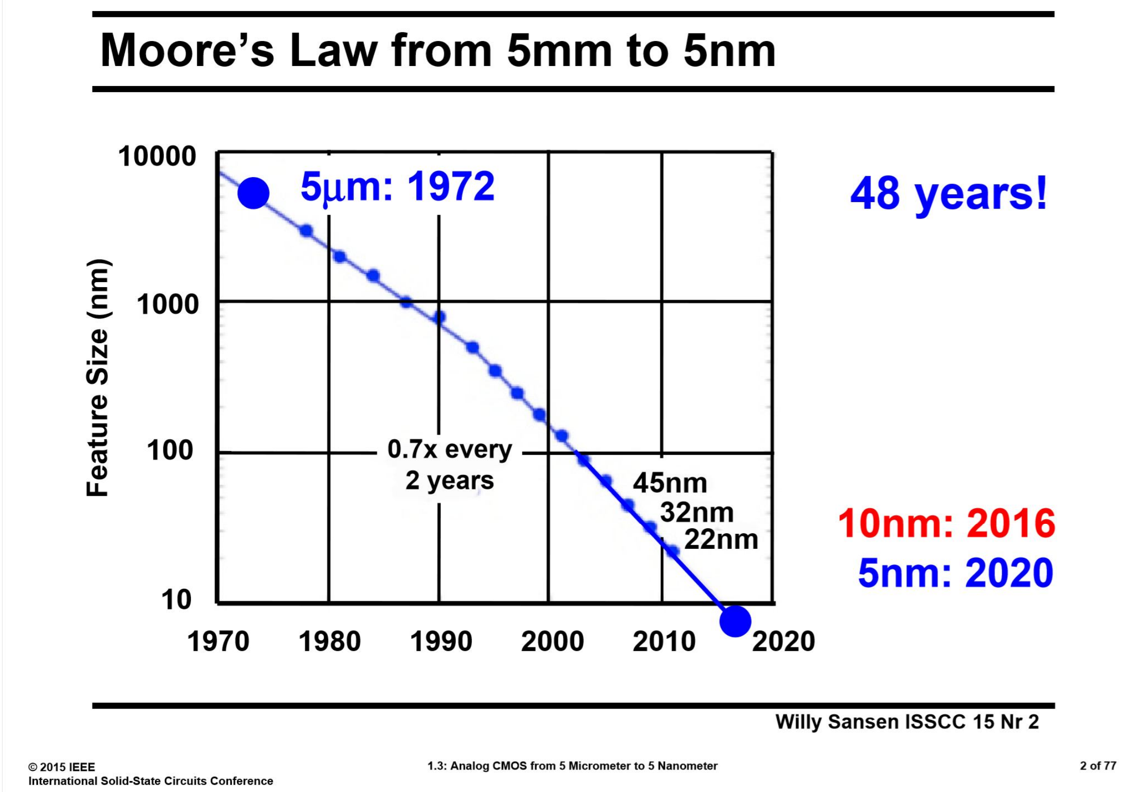

Technology Scaling – Moore – More than Moore

Our Expectation

Cray-1: world's fastest computer 1976-1982

- 64Mb memory (50ns cycle time)
- 40Kb register (6ns cycle time)
- ~1 million gates (4/5 input NAND)
- 80MHz clock
- 115kW

In 45nm (30 years later)

- < 3 mm^2
- > 1 GHz
- ~ 1 W

CRAY-1

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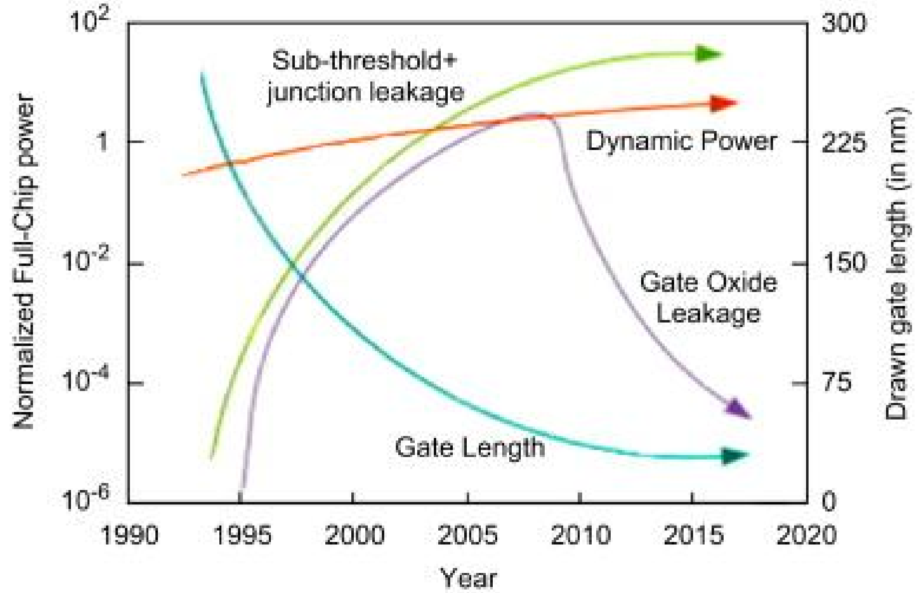
CMOS Technology Scaling

- Process scaling will continue
- Cost/transistor no longer reducing
- Energy density increasing
- Leakage currents increasing
- Mature process nodes here to stay
  - Driven by reliability requirements
  - Cost



Source: Z. Abbas, M. Oliveri "Impact of technology scaling on leakage power in nano-scale bulk CMOS digital standard cells" Microelectronics Journal

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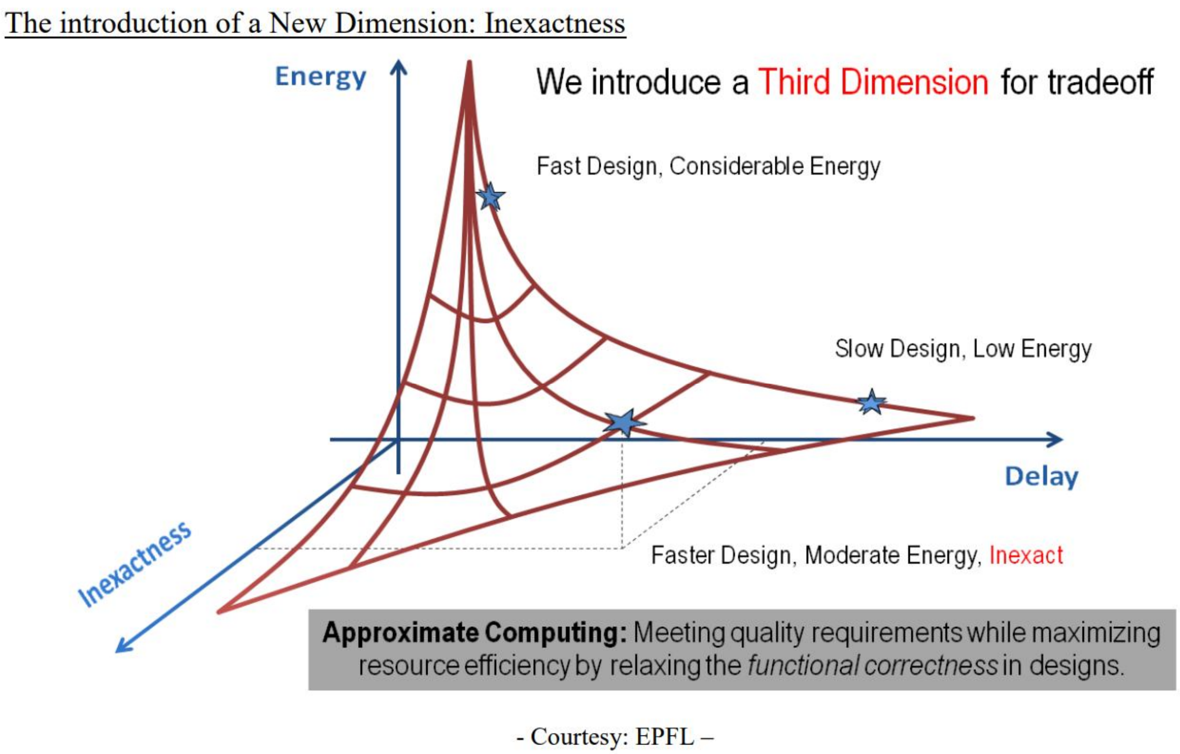
Adequate computing

- Full precision is not always required!
- Circuits / System
- Driven by QoS



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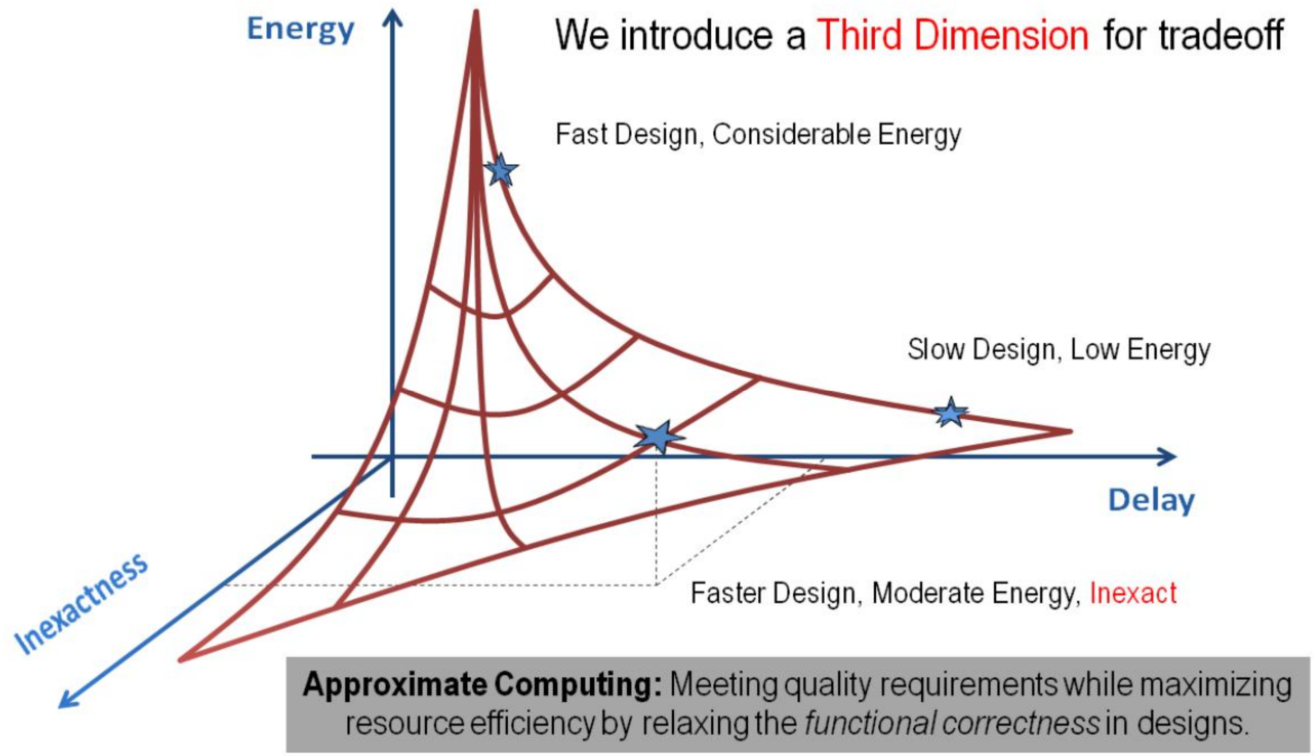
The introduction of a New Dimension: Inexactness



- Courtesy: EPFL –

Source: EU Workshop ““Energy-Efficient Computing Systems, dynamic adaptation of Quality of Service and approximate computing”

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Some recent developments

ISSCC 2018 / SESSION 17 / TECHNOLOGIES FOR HEALTH AND SOCIETY / 17.3

17.3 A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Employing a 180nW 64dB SNR Passive ΔΣ ADC and a 920MHz Wireless Transmitter

Ali Fazli Yeknami, Xiaoyang Wang, Somayeh Imani, Ali Nikoofard, Itthipon Jeerapan, Joseph Wang, Patrick P. Mercier

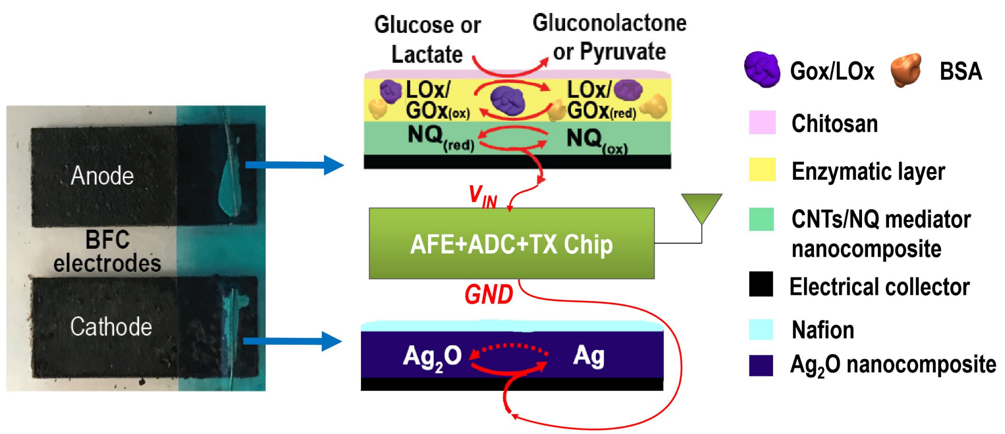
University of California, San Diego, La Jolla, CA

Wearable physiochemical biosensors offer an ex

or PMOS transistors, and are activated by a 3× clock booster (NMOS), or a -200mV charge pump (PMOS), as shown in Fig. 17.3.3 (top middle).

Output bits from the ΔΣM are passed through a *sinc*^{2} decimation filter, and stored in a FIFO until the TX is activated. The TX is designed as a single-stage direct-RF OOK-modulated power oscillator (RFPO) [6] that provides inherent impedance matching with a 1cm 920MHz on-board loop antenna (Fig. 17.3.4). Unfortunately, ... the start- ... npensate ... is design ... e voltage

BFC Material Composition



- BFC cathode material composition

Conclusions

- Significant progress in ULP design
- Energy Gap is reducing
- Most Power efficient block does not imply power efficient system
- Portfolio of tricks/techniques available
  - No silver bullet technique

Q & A

Thanks a lot for your time and attention!

Any questions and/or comments?

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