



AHEAD OF WHAT'S POSSIBLE™

Optimization of chip-scale thermoelectric energy harvesters for room temperature energy harvesting applications

EnerHarv 2018

J Cornett, H Berney, M Morrissey, S Haidar, M Dunham, S Geary, W Lane, B Chen

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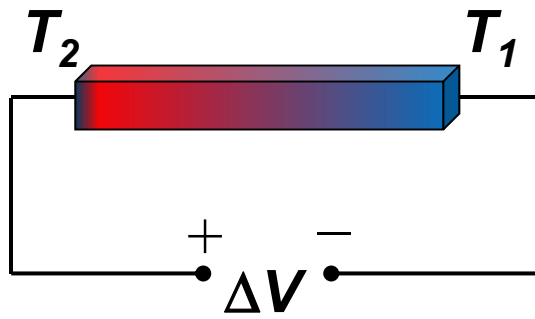
- ▶ Introduction to thermoelectricity
 - Thermoelectric effects
 - Refrigeration and power generation applications
 - Thermoelectric energy harvesting
- ▶ Design and modeling of TEGs
- ▶ ADI's chip-scale TEG
 - Device architecture
 - Process flow overview
- ▶ TEG-powered condition-based monitoring

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Thermoelectric Phenomena



Seebeck Effect



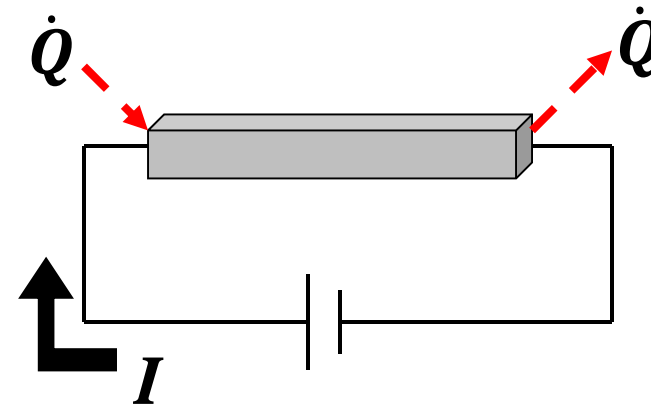
$$S = - \frac{\Delta V}{T_2 - T_1}$$

Seebeck coefficient

p-type: $S > 0$

n-type: $S < 0$

Peltier Effect



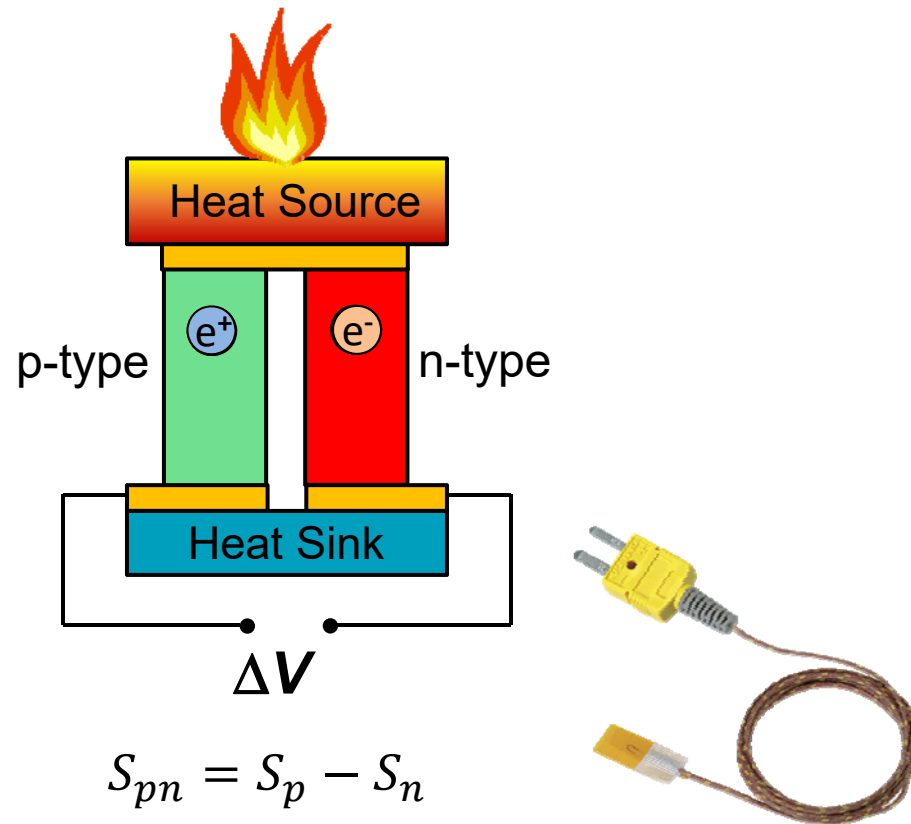
$$\pi = \frac{\dot{Q}}{I}$$

Peltier coefficient

p-type: $\pi > 0$

n-type: $\pi < 0$

Power Generation

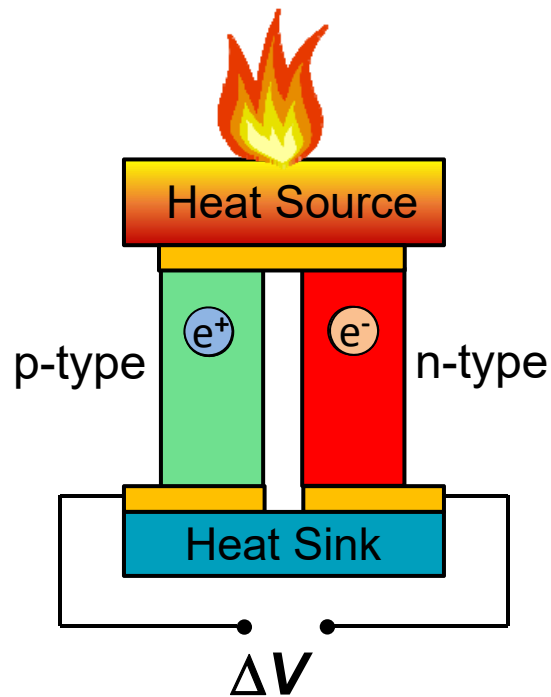


$$\begin{aligned} S_{pn} &= S_p - S_n \\ \Delta V_{pn} &= \Delta V_p - \Delta V_n \\ &= S_{pn} \cdot \Delta T \end{aligned}$$

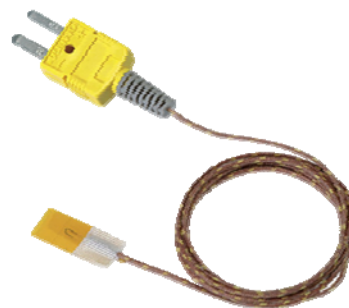
Thermoelectric Phenomena



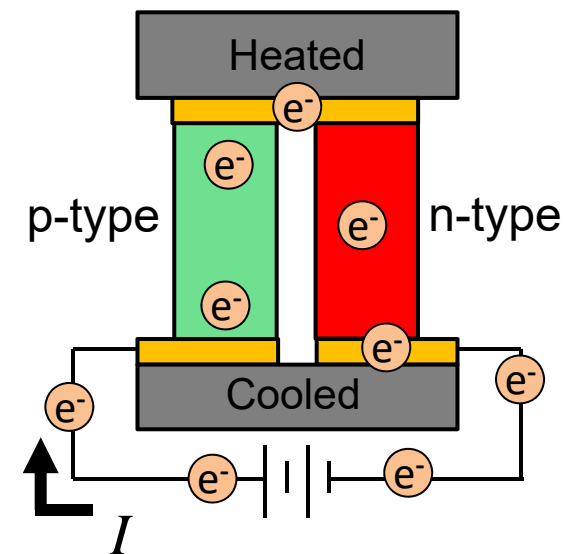
Power Generation



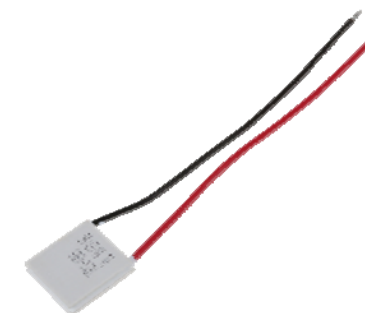
$$S_{pn} = S_p - S_n$$
$$\Delta V_{pn} = \Delta V_p - \Delta V_n$$
$$= S_{pn} \cdot \Delta T$$



Refrigeration



$$\pi_{pn} = \pi_p - \pi_n$$
$$\dot{Q}_{pn} = \dot{Q}_p - \dot{Q}_n$$
$$= \pi_{pn} \cdot I$$



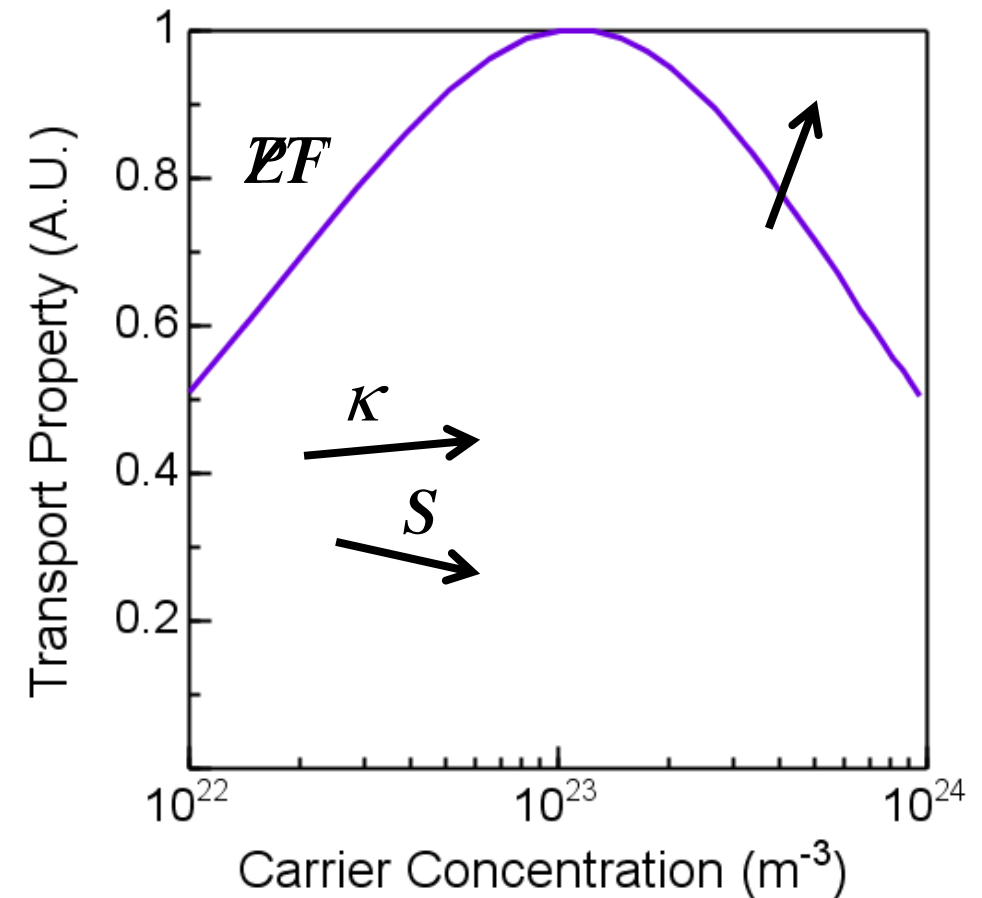
Thermoelectric Figure of Merit

$$ZT = \frac{\sigma S^2}{K} T$$

Maximize σS^2

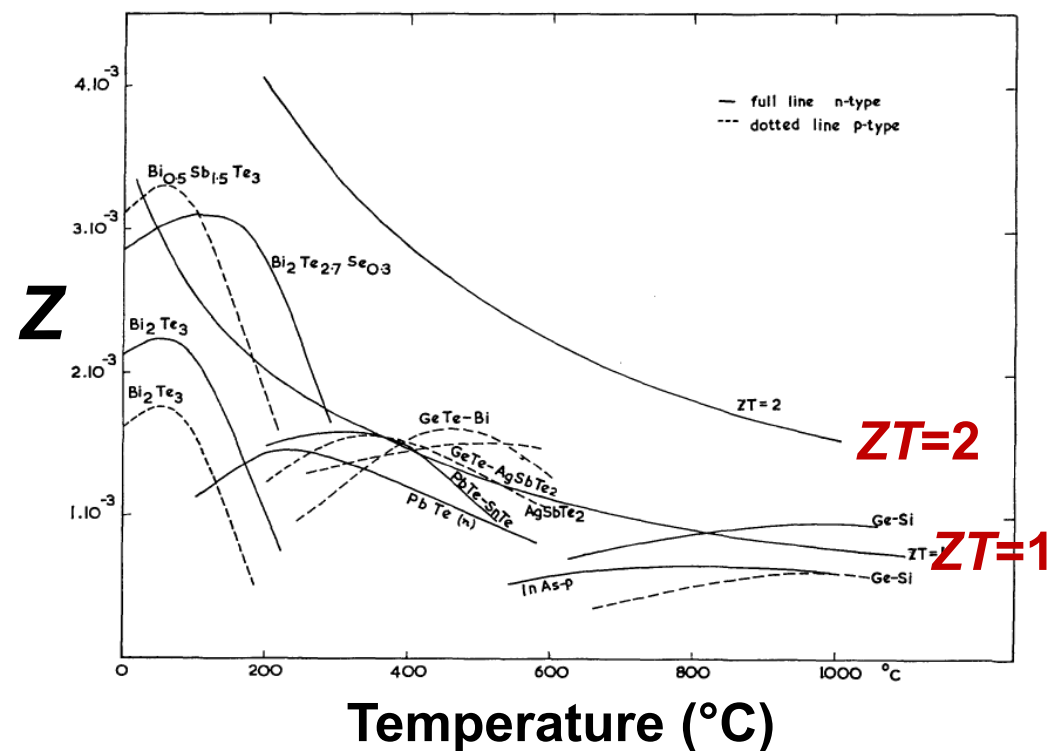
Minimize K

- σ : Electrical conductivity
 - S : Seebeck coefficient
 - σS^2 : Power factor
 - K : Thermal conductivity
- $K_e \propto \sigma$



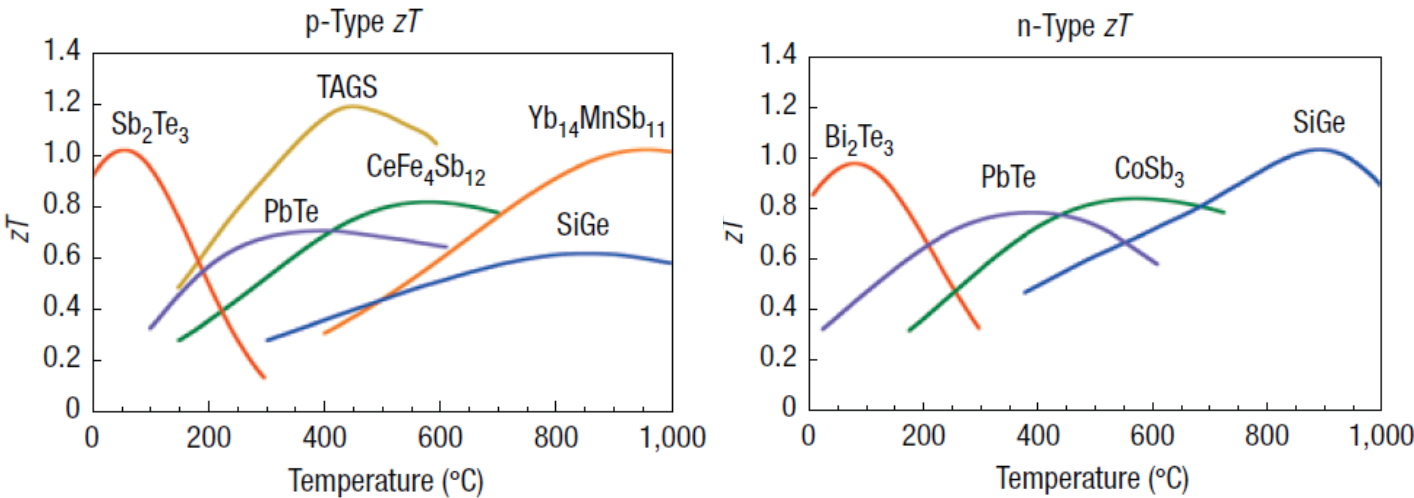
State-of-the-Art ZT Values

ZT in 1970



Wright, D.A. *Metallurgical Reviews* **15**, 147 (1970)

ZT in 2008



*Best room temperature
thermoelectric materials: Bi₂Te₃-
and Sb₂Te₃-related*

Snyder, G. et al. *Nature Mater.* **7**, 105-114 (2008)

Refrigeration Applications



CPU



Laser diodes



Picnic baskets



Car seats



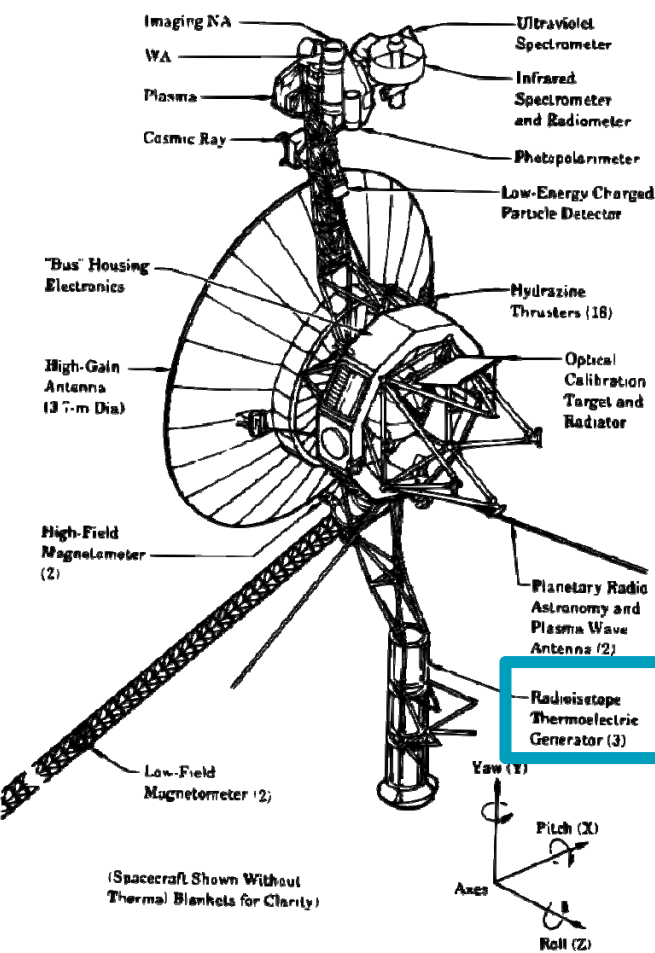
Wine coolers

Power Generation Applications



In Space

Voyager (1977-?)



Galileo (1989-?)



Mars Rover Curiosity (2011-?)

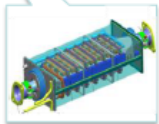
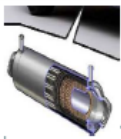
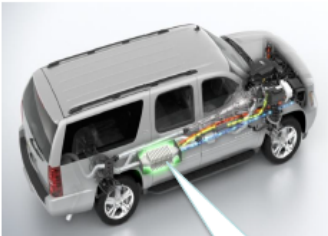


On Earth

Ford Lincoln MKT



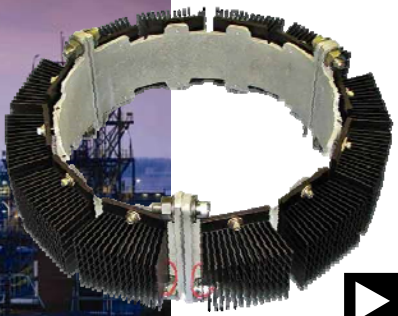
Chevy Suburban



BMW X6



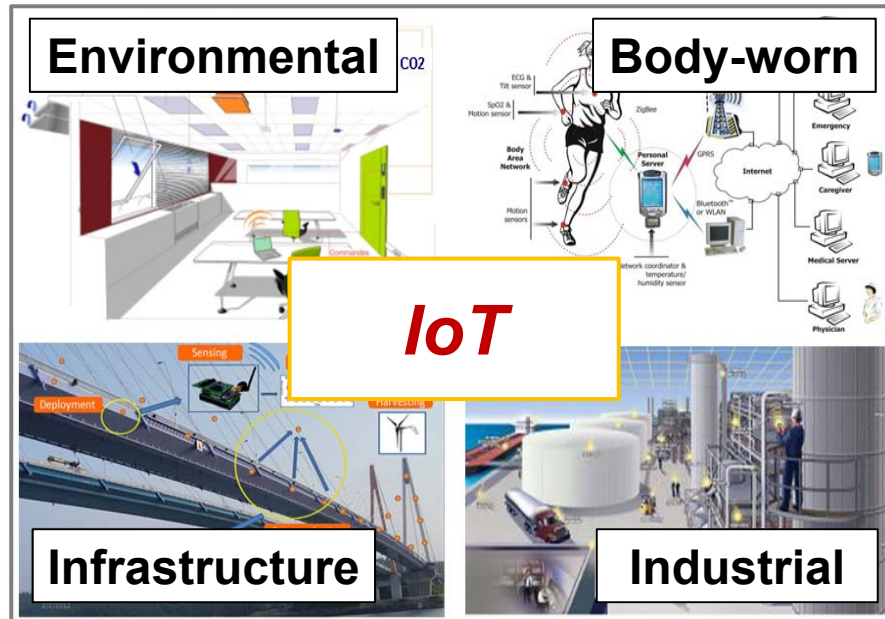
Marlow PowerStrap



Power Generation Applications: The Internet of Things



- **Problem:** Continuously growing market of small wireless devices and sensors require power



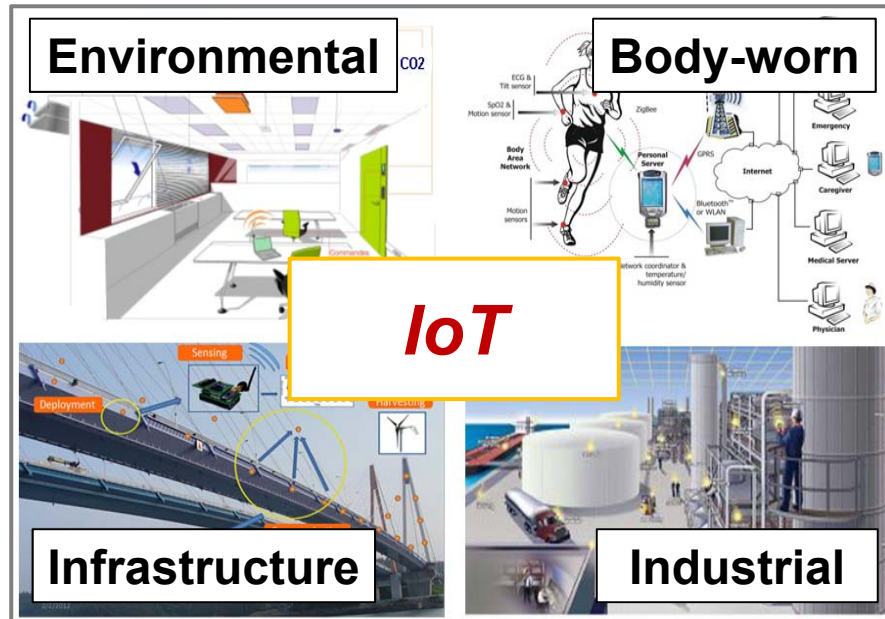
Power Generation Applications: The Internet of Things



- **Problem:** Continuously growing market of small wireless devices and sensors require power

- **Solution:** Energy harvesting

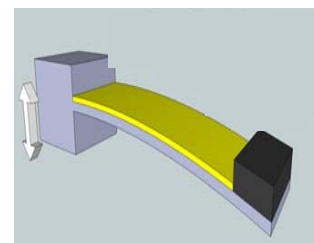
Generating small amounts of power from external, otherwise wasted sources



Solar



Wind



Vibration



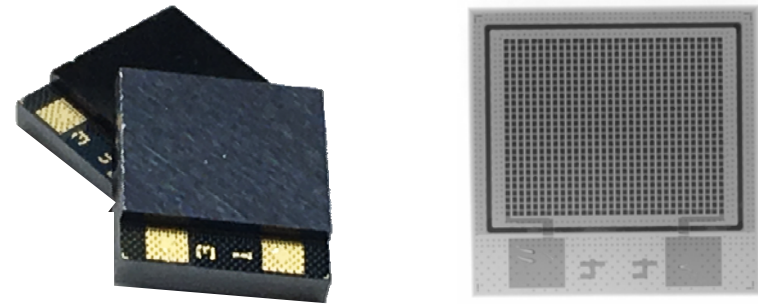
Heat

**Thermoelectric
energy harvesting!**

Chip-Scale Thermoelectric Energy Harvesting



VS



Bulk TEG

- Large device area
- Expensive
- Bulk processing: Low number of TE legs
- Low device thermal resistance
- Low output voltage

Chip-scale TEG

- Small device area (**10mm²**)
- Low-cost
- Microfabrication: Hundreds to thousands of TE legs
- High device thermal resistance: **Optimize ΔT captured**
- High output voltage: **Maximize efficiency** of power management

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Design of Chip-Scale TEGs

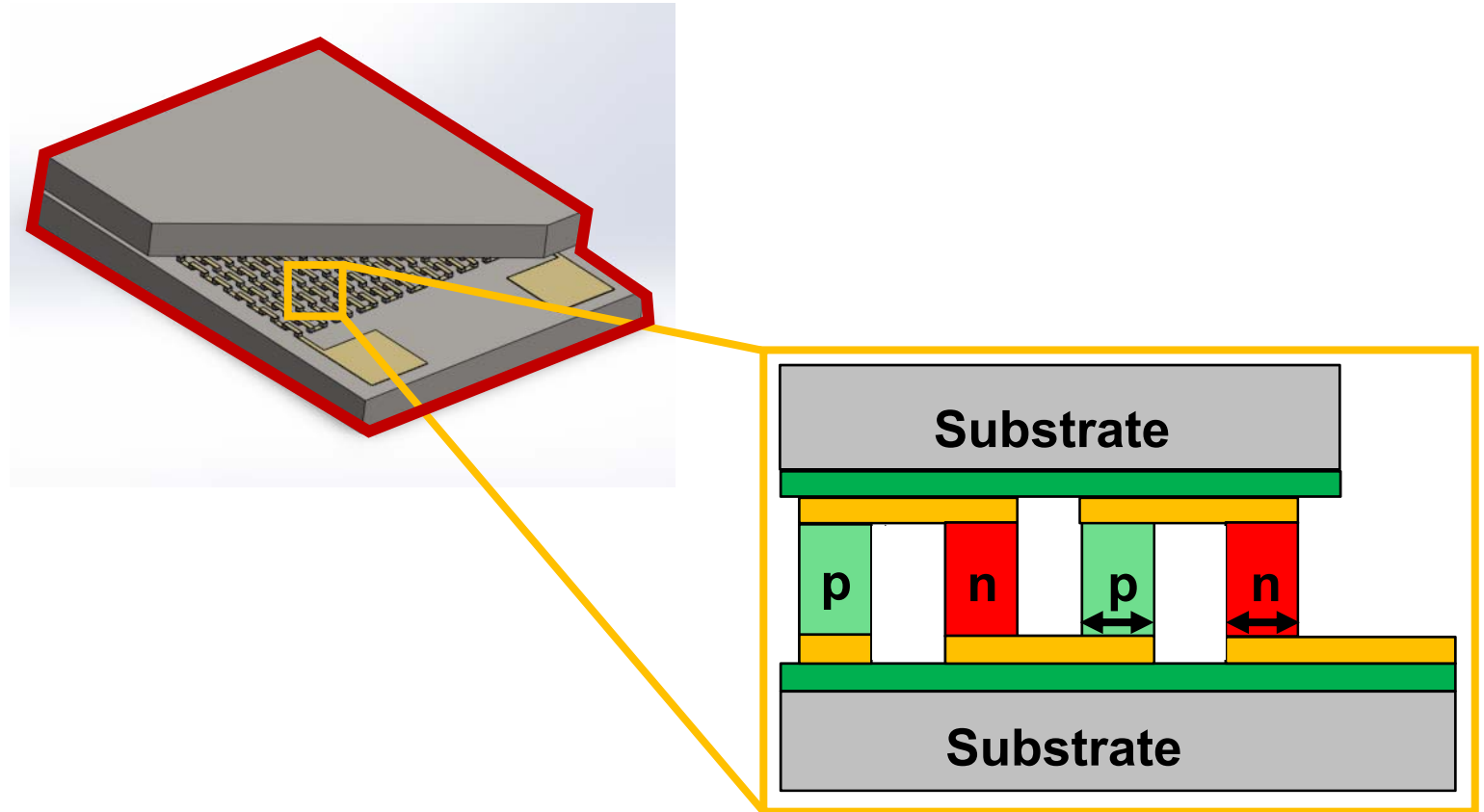


► **Design parameters:**

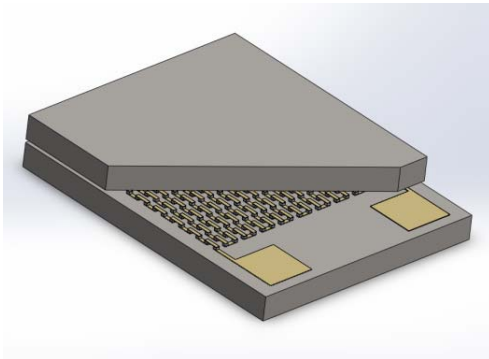
- Total device area
- Substrate material and thickness
- TE materials
- Interconnect materials
- TE element height
- TE element area
- Number of TE elements (fill factor)
- Filler material

► **Device characteristics:**

- Electrical resistance
- Thermal resistance
- Output voltage (device Seebeck)



Modeling of Chip-Scale TEGs

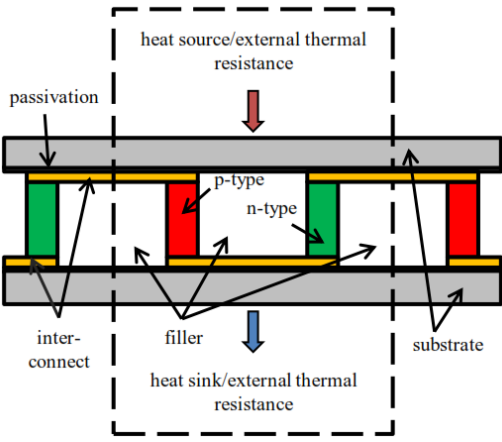


Complete TEG

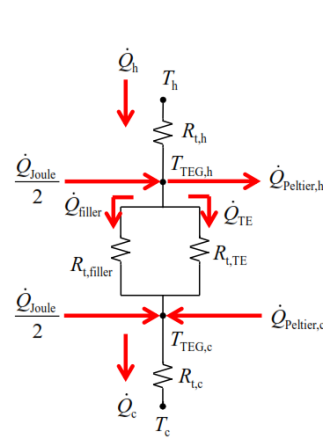
Modeling of Chip-Scale TEGs



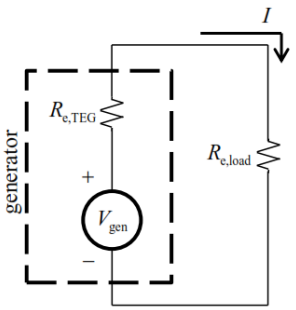
Complete TEG



Simplify thermal and electrical systems:
Single Thermocouple



1D thermal resistor network



$$P_{load} = \frac{V_{load}^2}{R_{load}} \propto (\Delta T_{TEG})^2$$

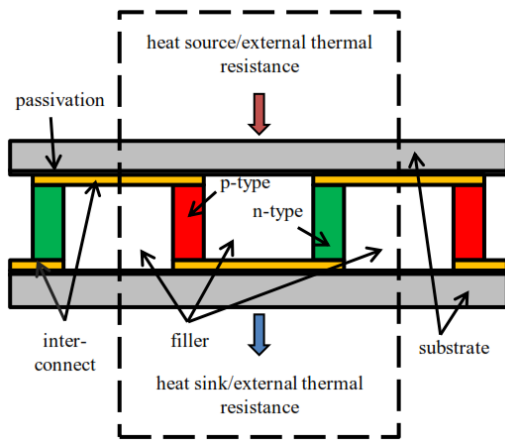
Simplified electrical circuit

Dunham, et al., 2015, Energy

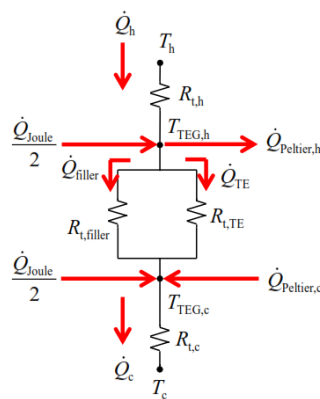
Modeling of Chip-Scale TEGs



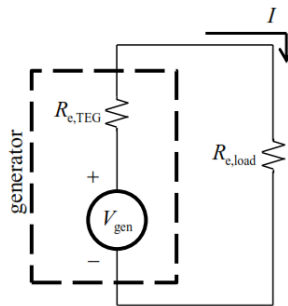
Complete TEG



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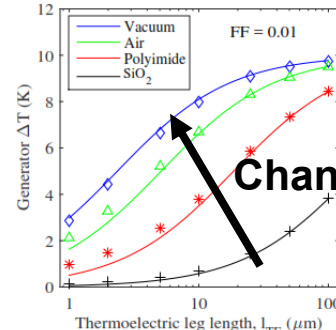
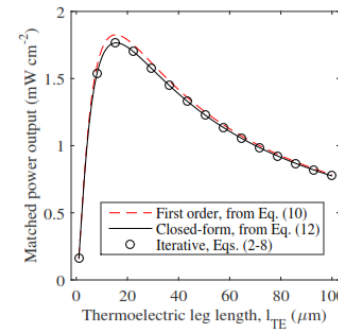
Simplified electrical circuit

Performance Matrix

Change # of TCs

DEVICE THERMAL RESISTANCE - 25 W

Leg Wt μm	T.A. Power mW	FF %	Device T.A. Power mW	Package Power mW	Power mW	Power mW	Power mW	Power mW
20	4.99	1668	10	2040	804	1.39	0.58	2400
20	4.99	1668	10	2040	367	0.86	0.38	2500
20	4.99	1668	12	2040	288	0.85	0.34	2500
20	4.99	1668	15	2040	209	0.72	0.29	2500
20	4.99	1668	20	2040	135	0.58	0.23	2500
20	4.99	1668	30	2040	70	0.43	0.16	2600
19	4.99	1668	4	2040	977	1.7	0.81	2700
19	4.99	1668	10	2040	871	1.75	0.85	2700
19	4.99	1668	15	2040	779	1.75	0.77	2700
19	4.99	1668	18	2040	711	1.73	0.73	2700
19	4.99	1668	20	2040	675	1.69	0.71	2700
19	4.99	1668	25	2040	52	0.75	0.67	2800



Change filler

Change leg length

Excellent 1st approximation for expected device performance

Modeling of Chip-Scale TEGs

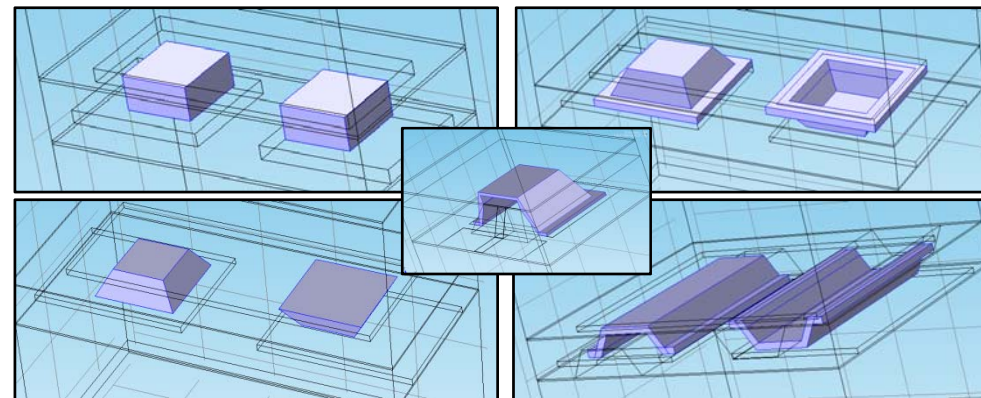
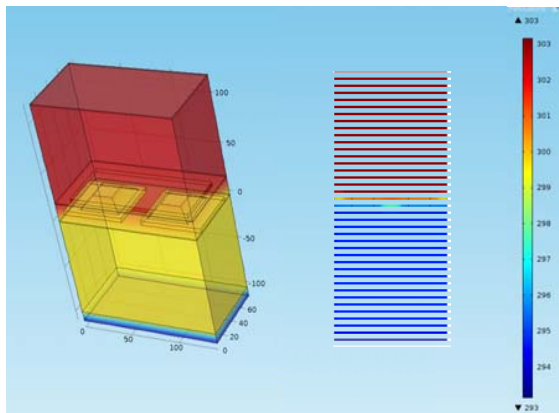
Using 3D finite elemental analysis software



Complete TEG

3D FEA Modeling (COMSOL)

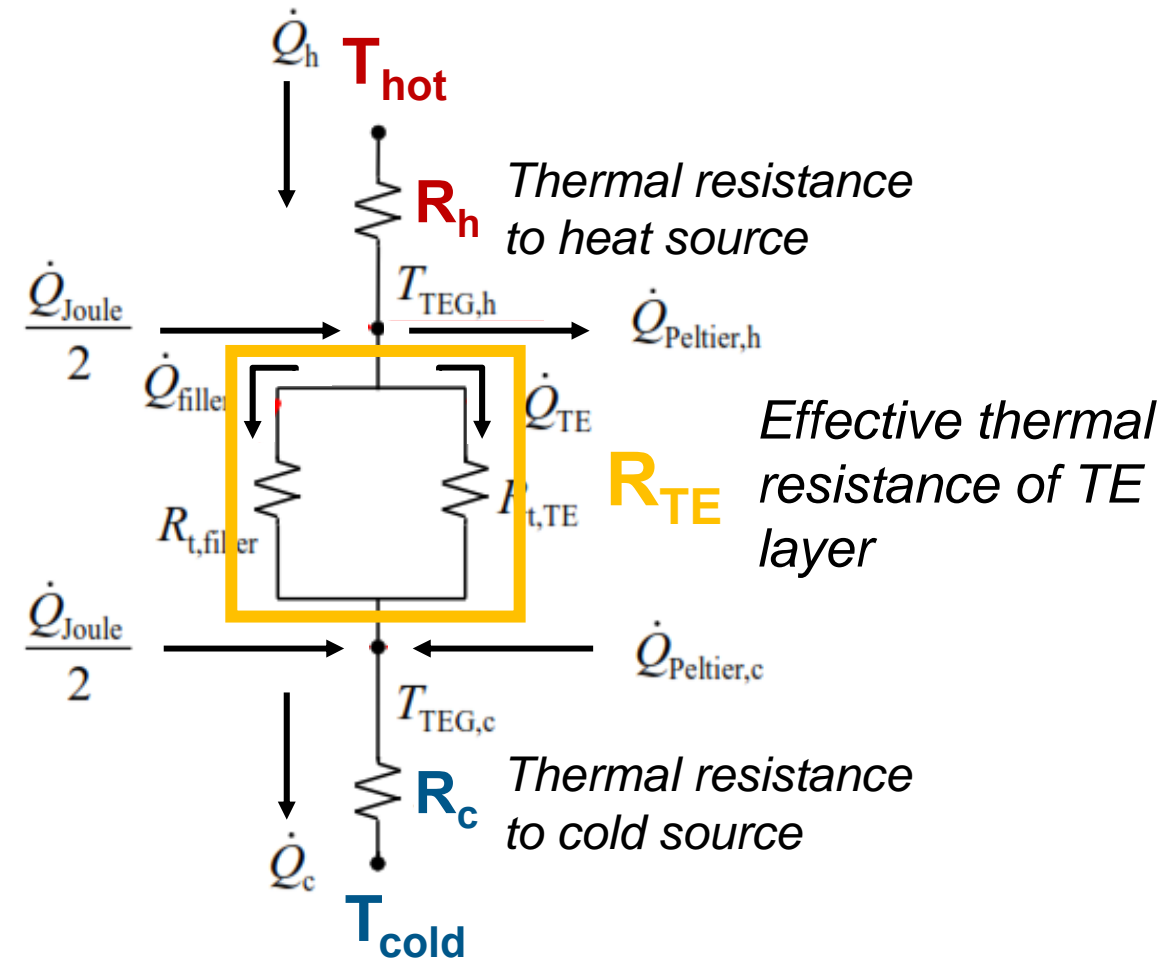
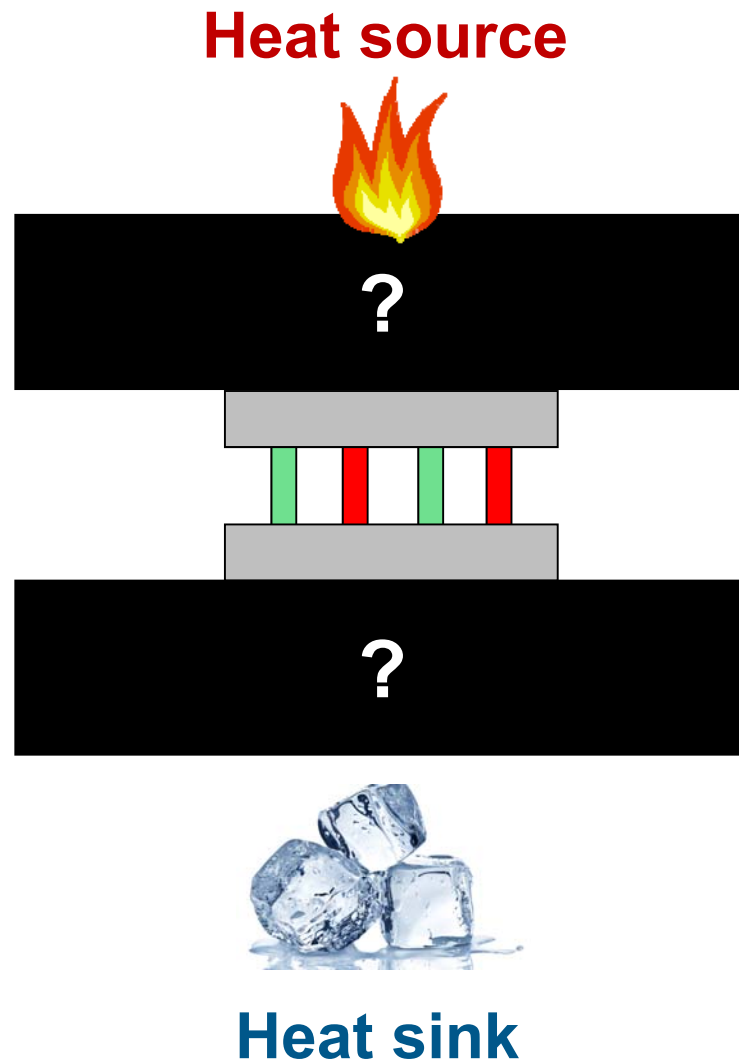
- *Fine-tune device performance*
- *Explore 3D adjustments to geometry*
- *Elucidate problem areas*



Simplify thermal and electrical systems: Single Thermocouple

Important Design Constraint

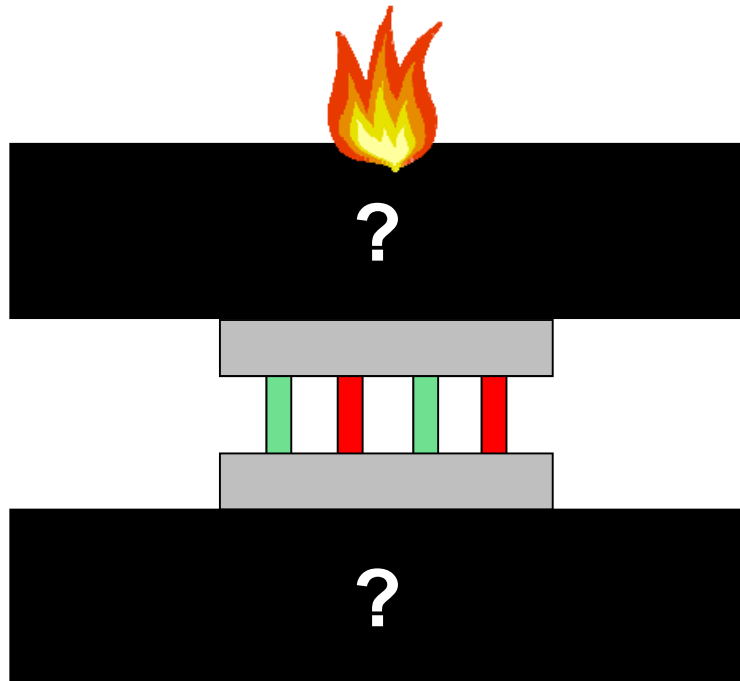
Thermal resistance of TEG



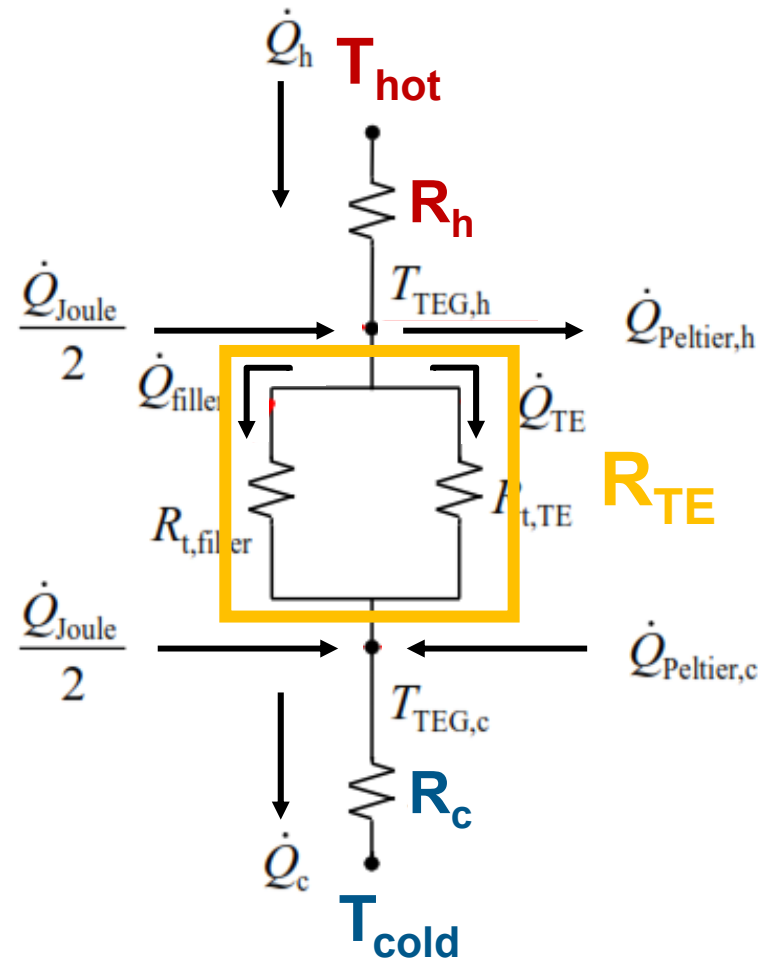
Important Design Constraint

Thermal resistance of TEG

Heat source



Heat sink



Condition for Maximum Power Output

$$R_{TE} = R_h + R_c$$

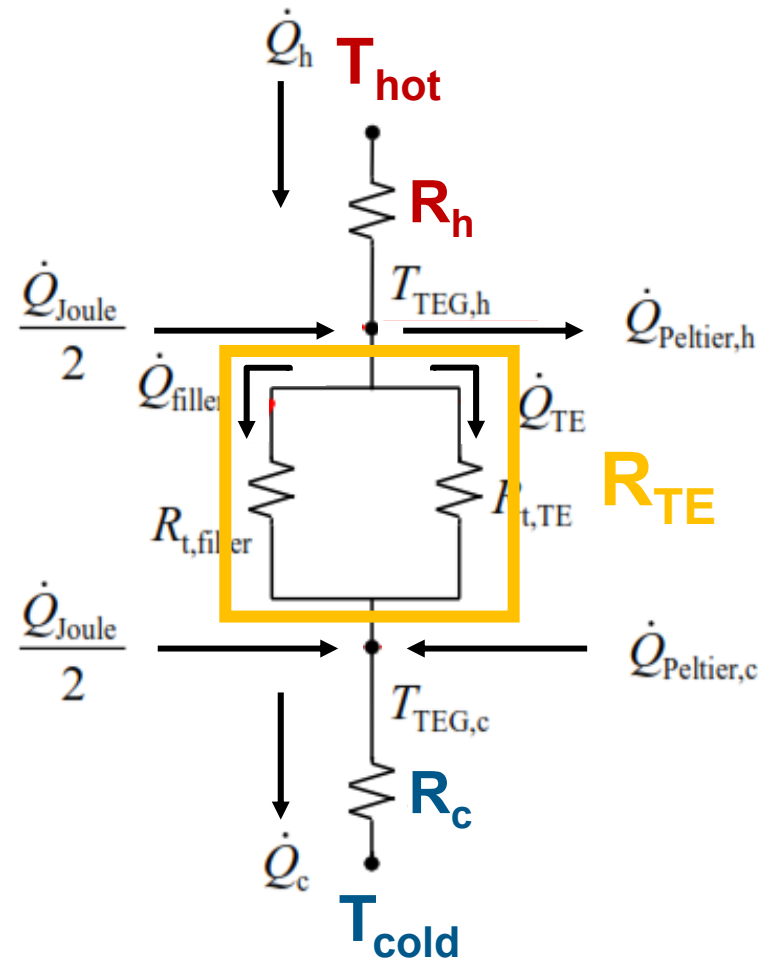
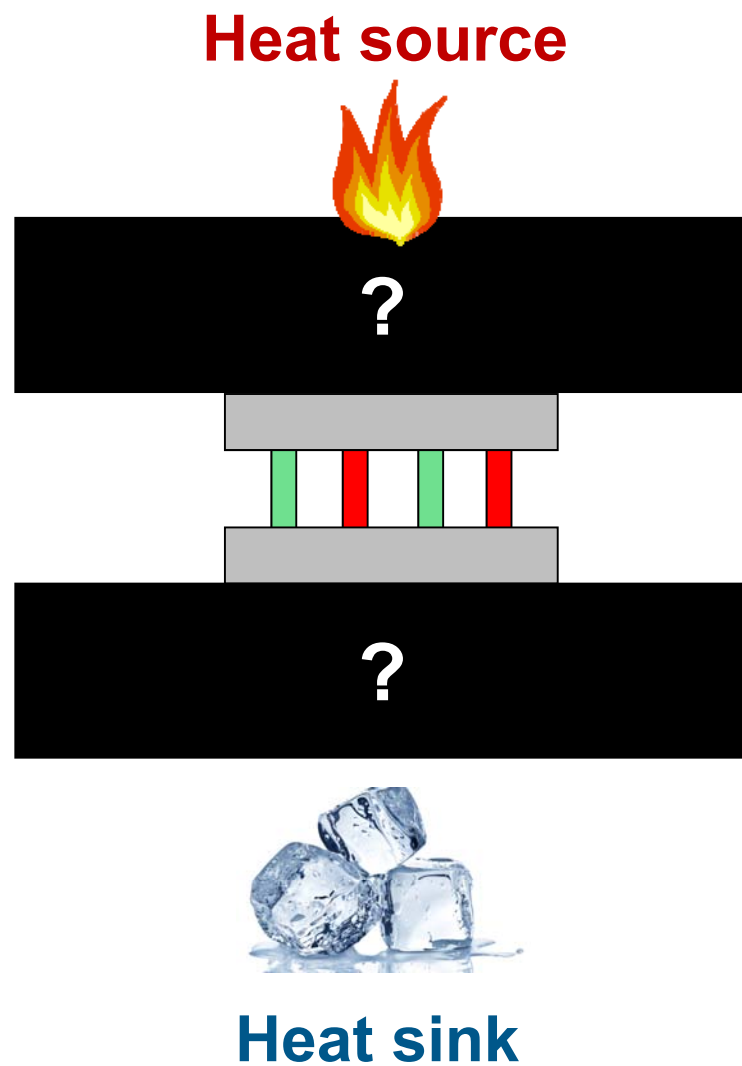
Thermal impedance matching

$$\Delta T_{TE} = \frac{T_h - T_c}{2}$$

Half of total ΔT falls across TE

Important Design Constraint

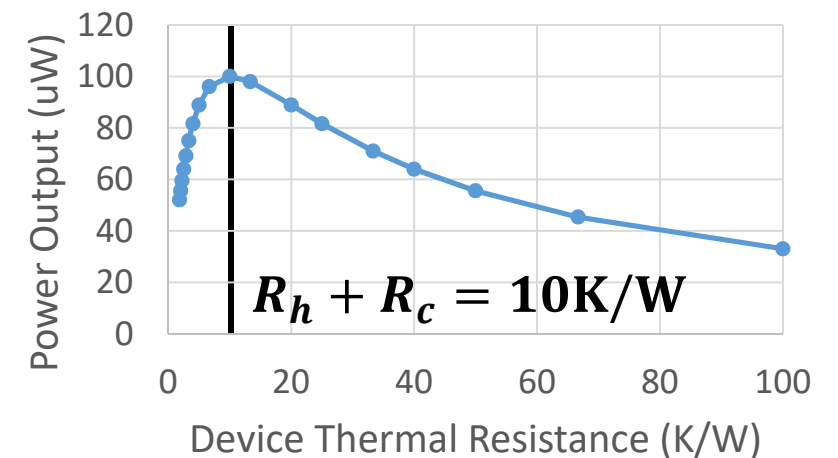
Thermal resistance of TEG



Condition for Maximum Power Output

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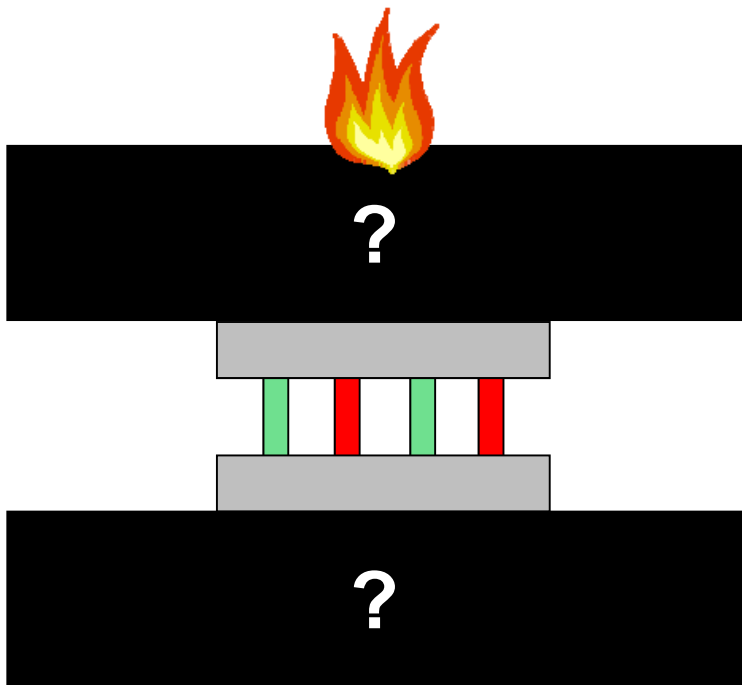
Thermal impedance matching



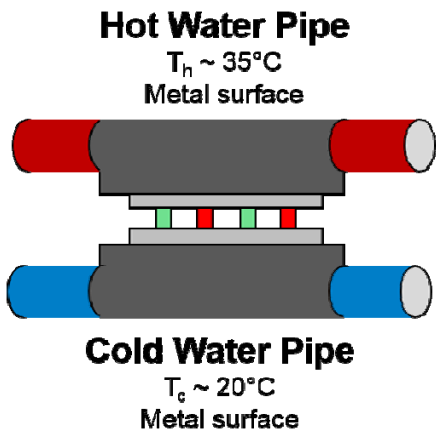
**** Max power will shift to lower device resistances with inclusion of Peltier, Joule effects ****

Representative Values for R_h , R_c

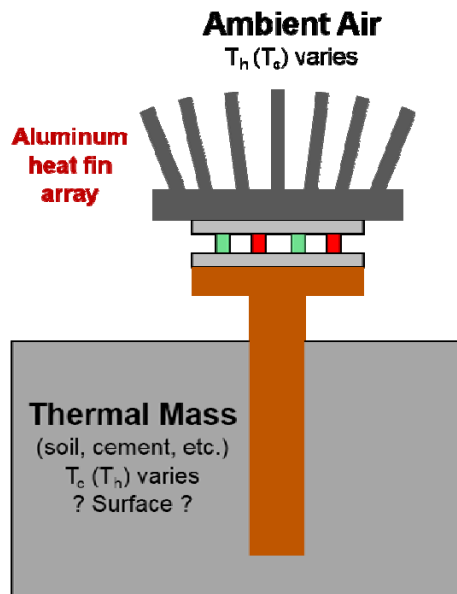
Heat source



Heat sink

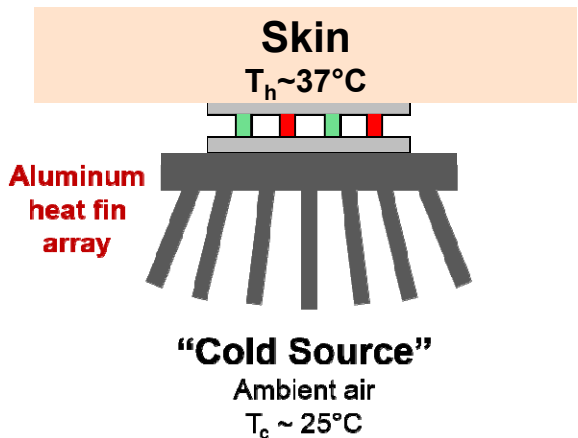
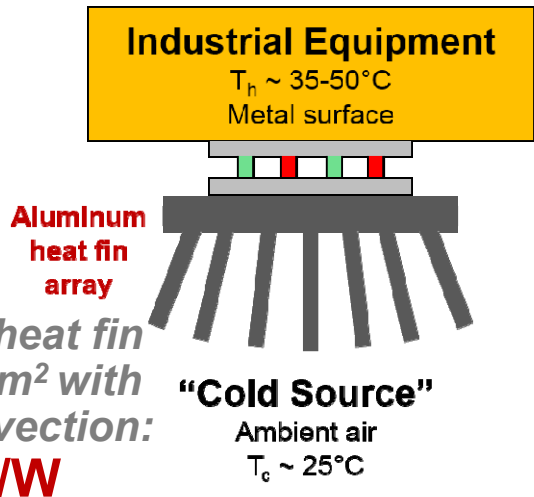


*Metal-to-metal
contact with thermal
adhesive or grease:*
 $\sim 1 \text{ K/W}$



*Skin contact w/ 4cm
diameter watch face:*
 $\sim 50 \text{ K/W}$

*Contact via heat pipe
to thermal mass:*
 $?? \text{ K/W}$
 (depends highly on
materials and time-
dependent temperatures)



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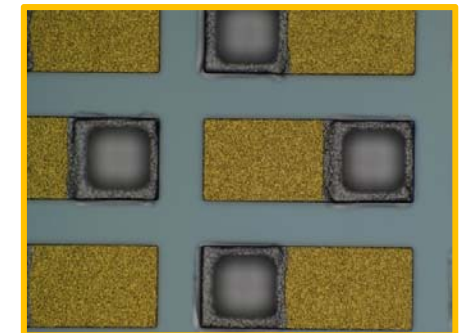
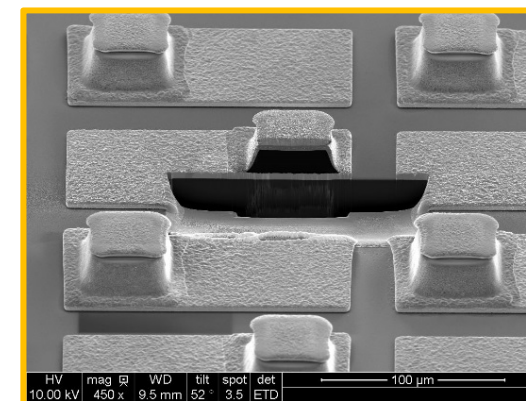
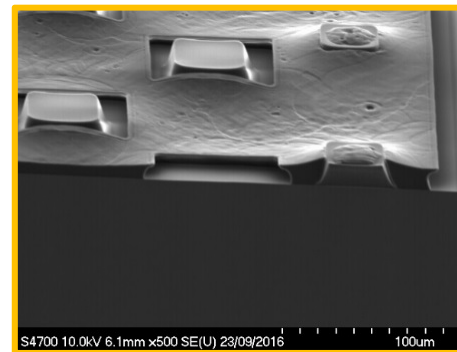
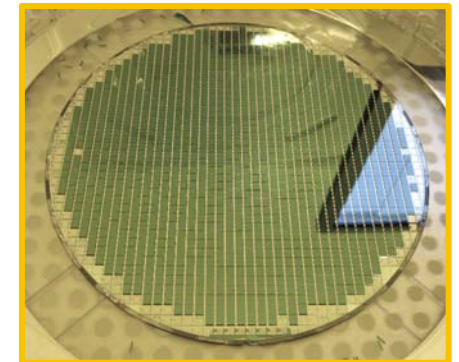
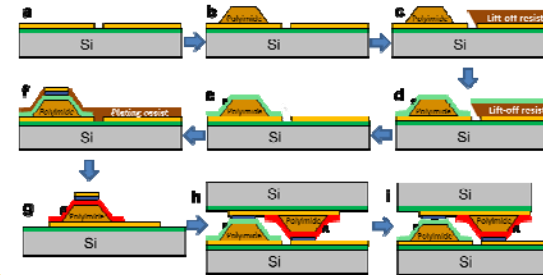
ADI Chip-Scale Thermoelectric Generator (TEG)



- Leveraging ADI manufacturing and processing know-how to build high-performance, low-cost devices
 - Target: **400 μ W from $\Delta T=10^{\circ}\text{C}$**



In-house 8" wafer processing



ADI Chip-Scale Thermoelectric Generator (TEG)



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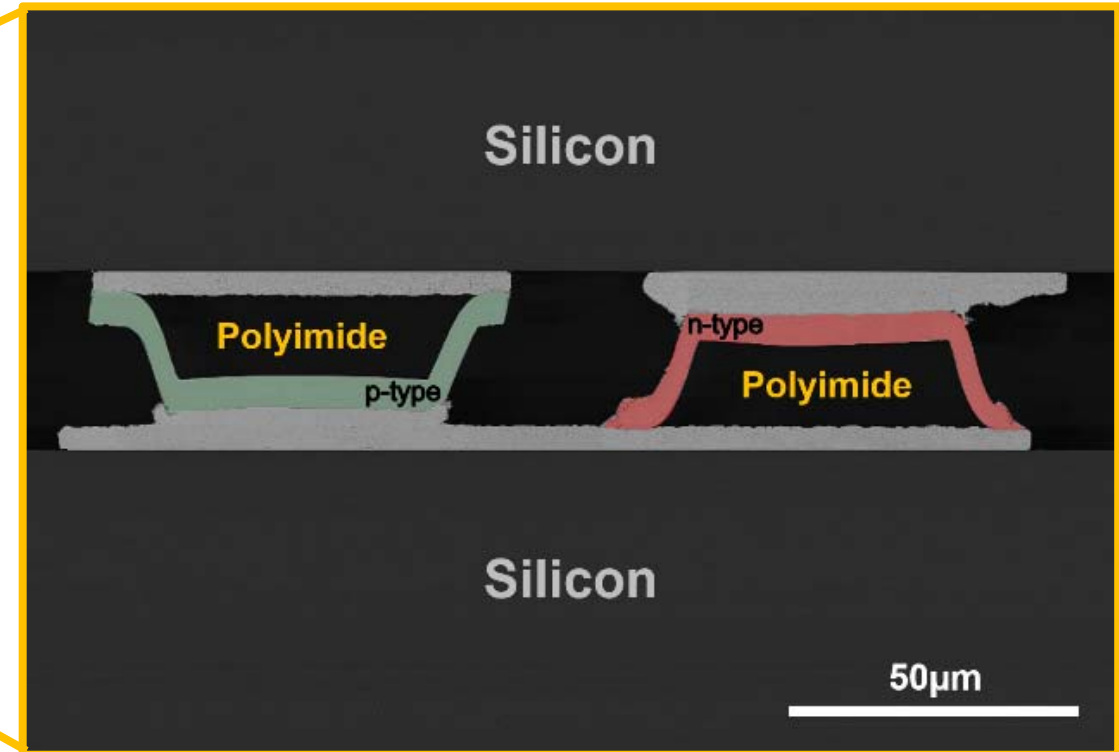
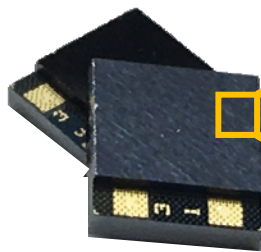
- Chip-scale device area: **$\sim 10\text{mm}^2$**

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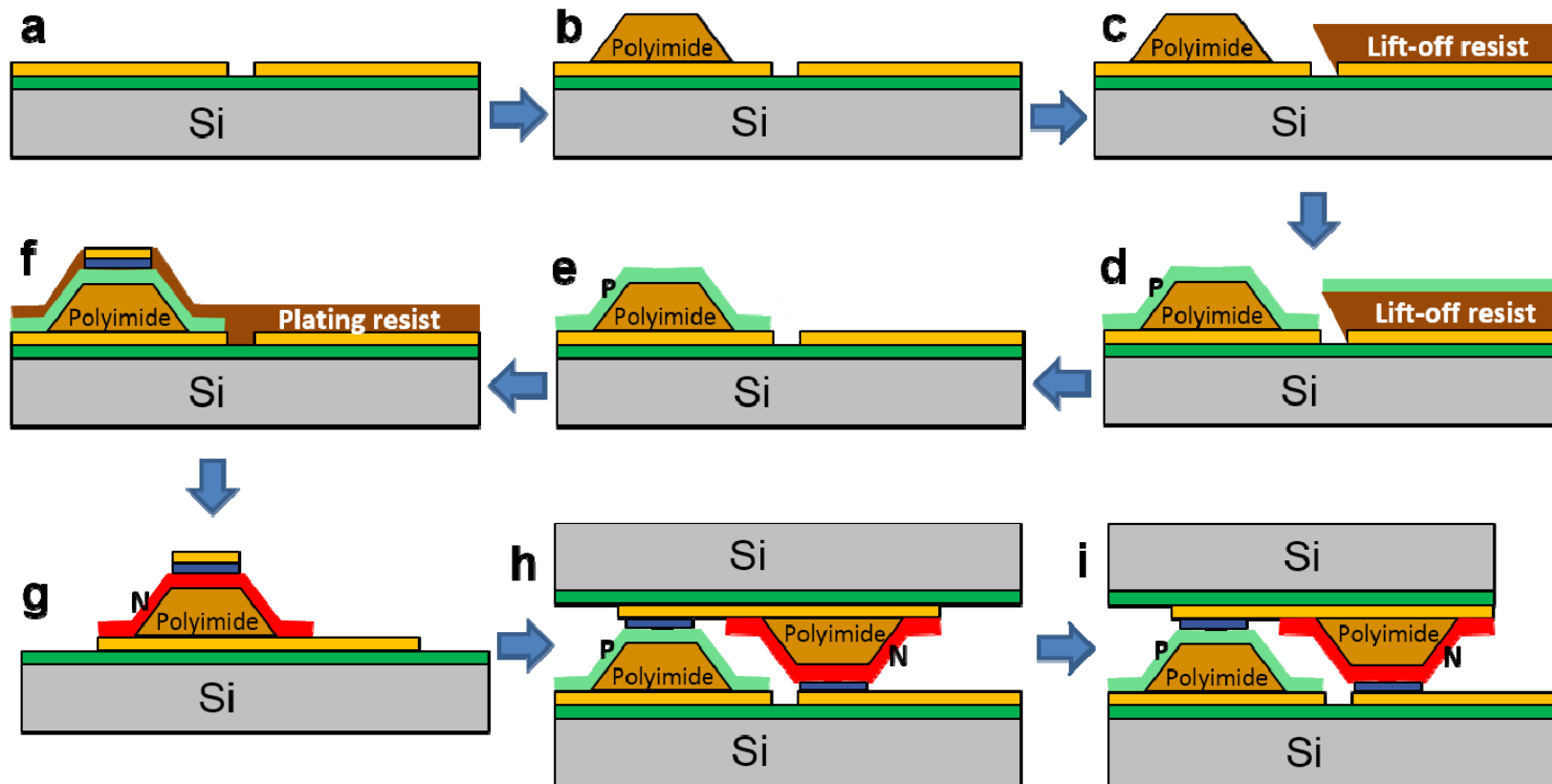
- Target: **400 μ W from $\Delta T=10^{\circ}\text{C}$**



Optimized to power wireless sensor nodes and other small devices from thermal energy sources close to room temperature

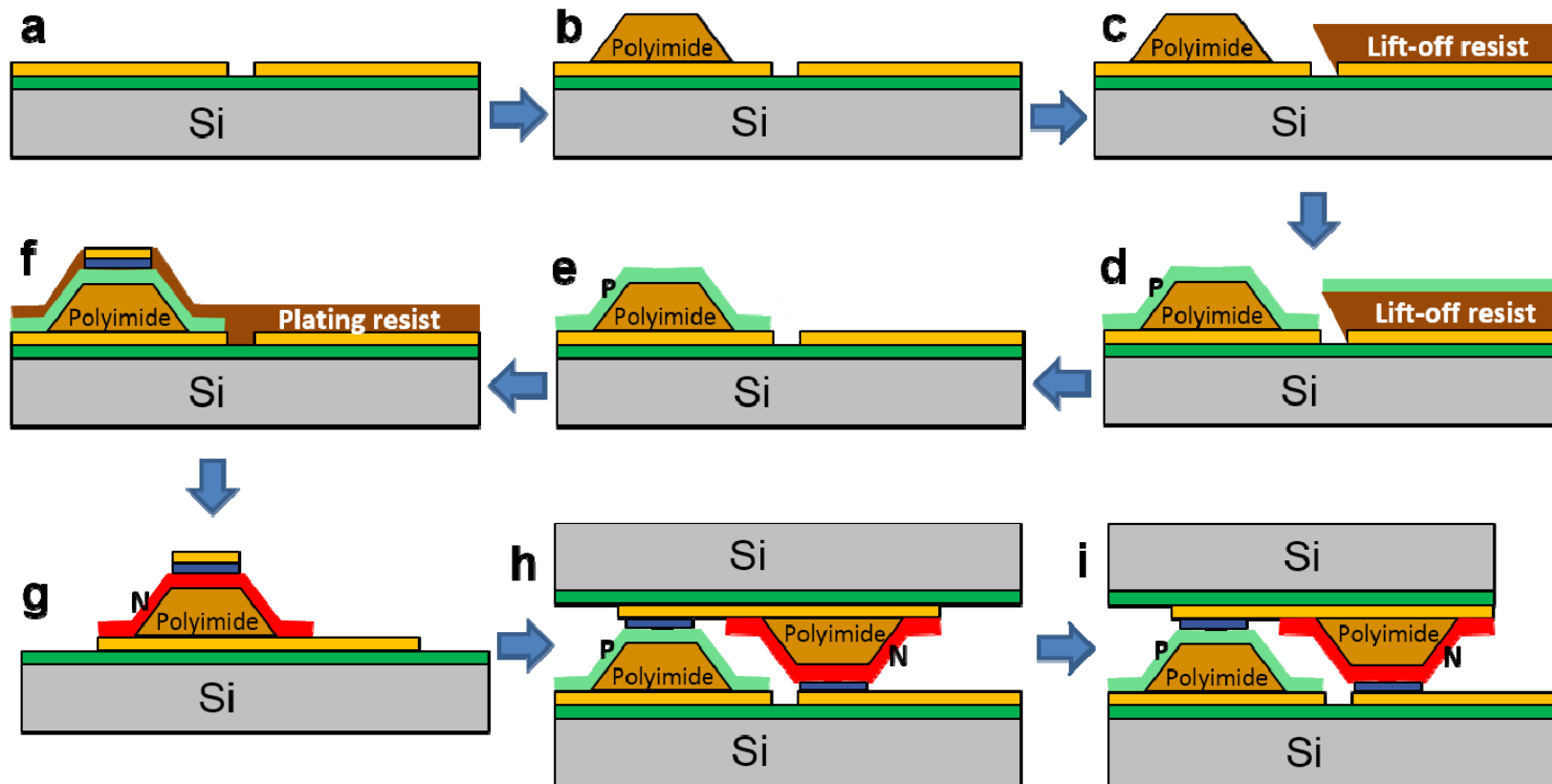
- Chip-scale device area: **$\sim 10\text{mm}^2$**
- Active materials: **Based on Bi_2Te_3**
- Make use of ADI-patented device architecture: **TE materials deposited along polyimide slope**
- Long leg length, large thermal resistance without time-consuming, expensive depositions

Process Flow for ADI Chip-Scale TEG



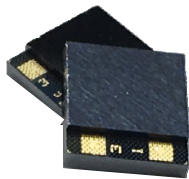
- a. Plating of interconnect
- b. Polyimide deposition
- c. Lift-off resist litho
- d. Bi_2Te_3 (Sb_2Te_3) deposition
- e. Lift-off
- f. Plating resist litho
- g. Plating of bond materials
- h. Wafer-level bond
- i. Singulation and dicing

Process Flow for ADI Chip-Scale TEG



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Projected Performance of ADI Chip-Scale TEG

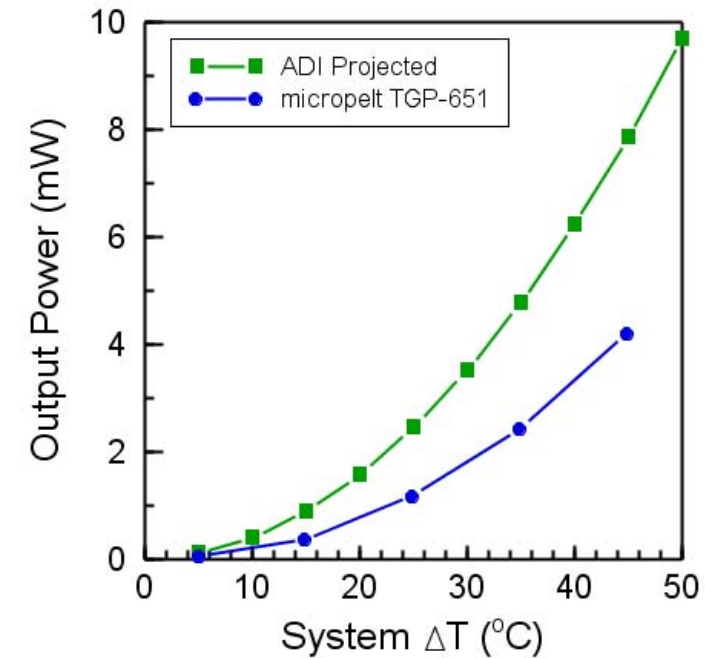
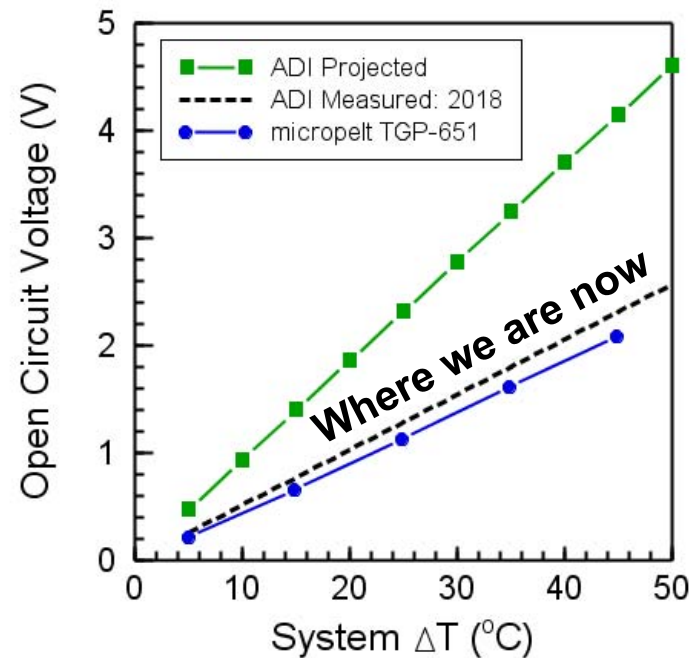
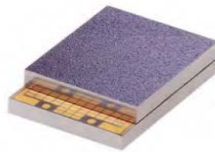


ADI TEG
Projected
performance

Performance compared with:

**micropelt
TGP-651**

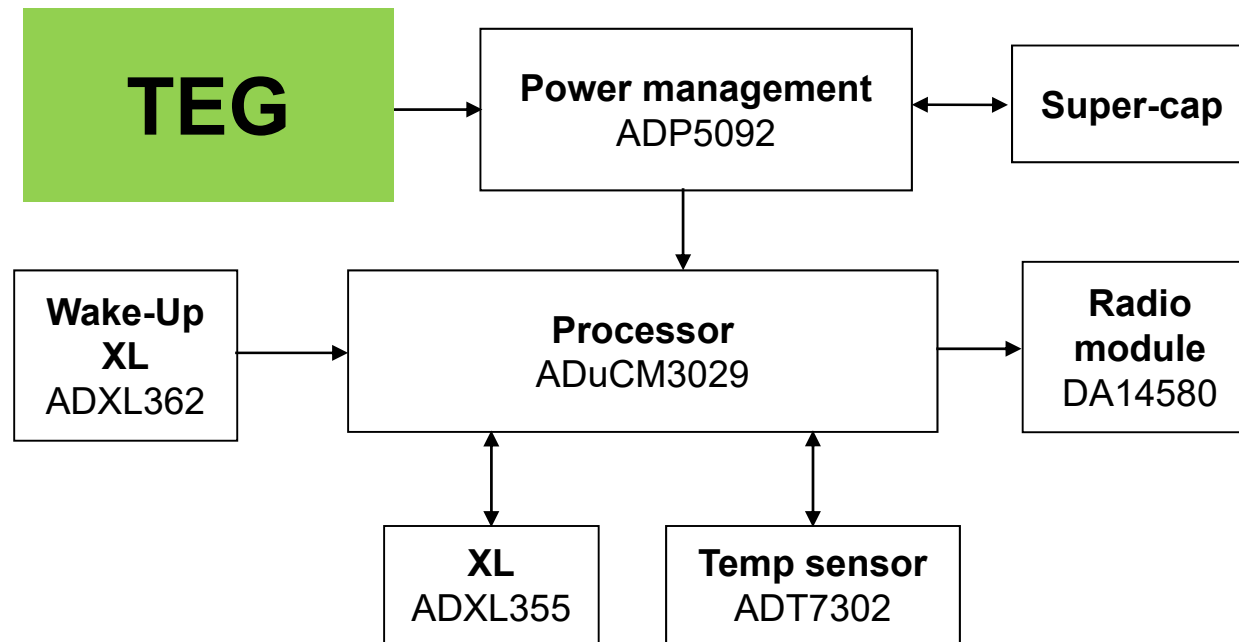
- Bi₂Te₃-based
- 3mm x 3mm



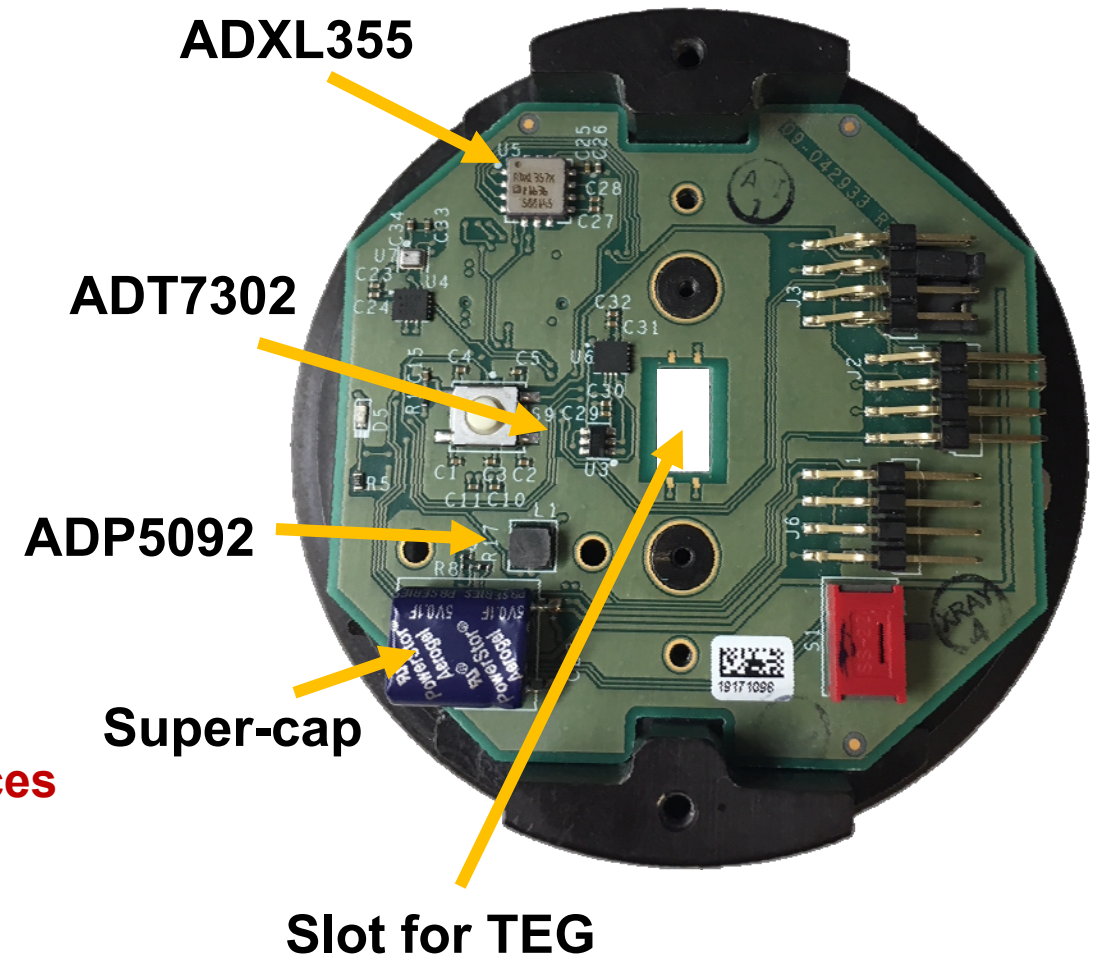
- ▶ **ADI TEGs predicted to have better performance (higher voltage and higher output power) than competitor**
 - Measured output voltage already surpasses Micropelt
 - *Resistance and power output improvements ongoing*
- ▶ **Schedule for sampling:**
 - 1st gen. prototypes: **Completed May 2017**
 - Customer sampling: **Summer 2018**

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TEG-Powered CbM Sensor Node



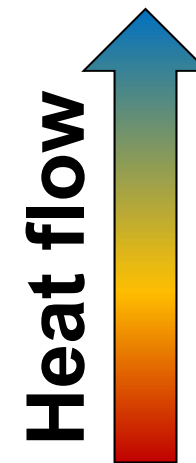
- ANALOG DEVICES **components**
 - ADuCM3029 microcontroller: SPI, I²C, UART interfaces
 - Ultra-low power ADP5092 power management
 - Low power vibration (ADXL263, ADXL355) and temperature (ADT7032) sensors



TEG-Powered CbM Sensor Node



TEG

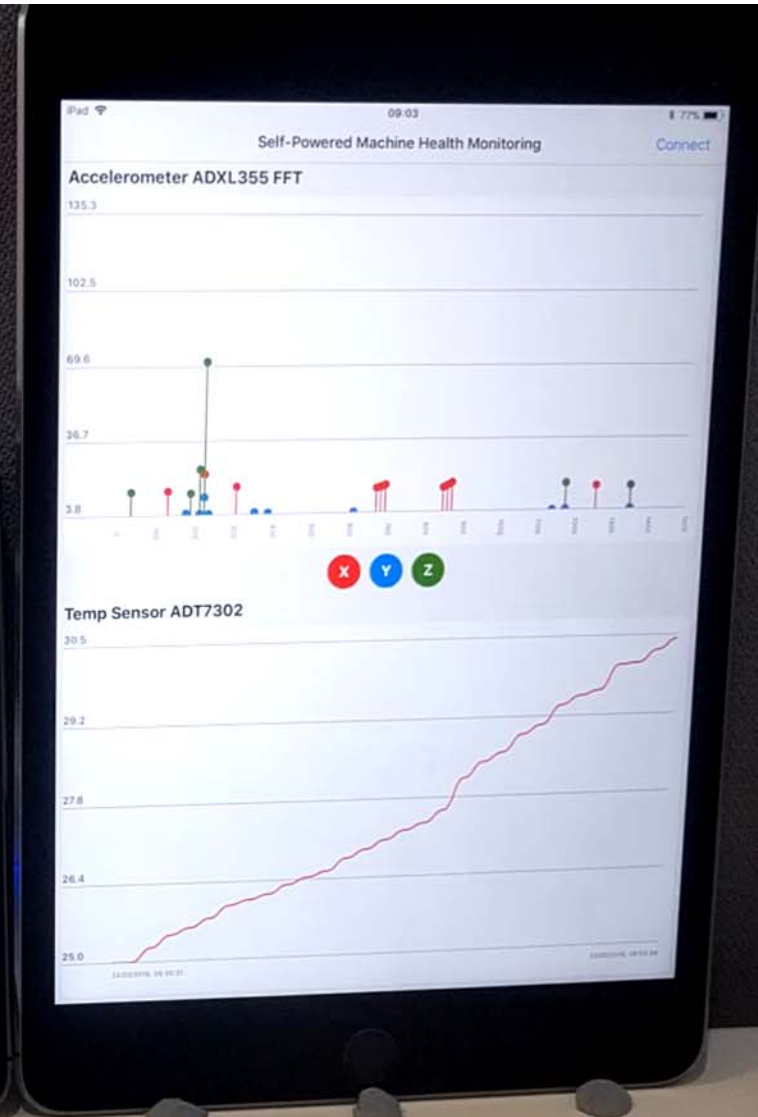
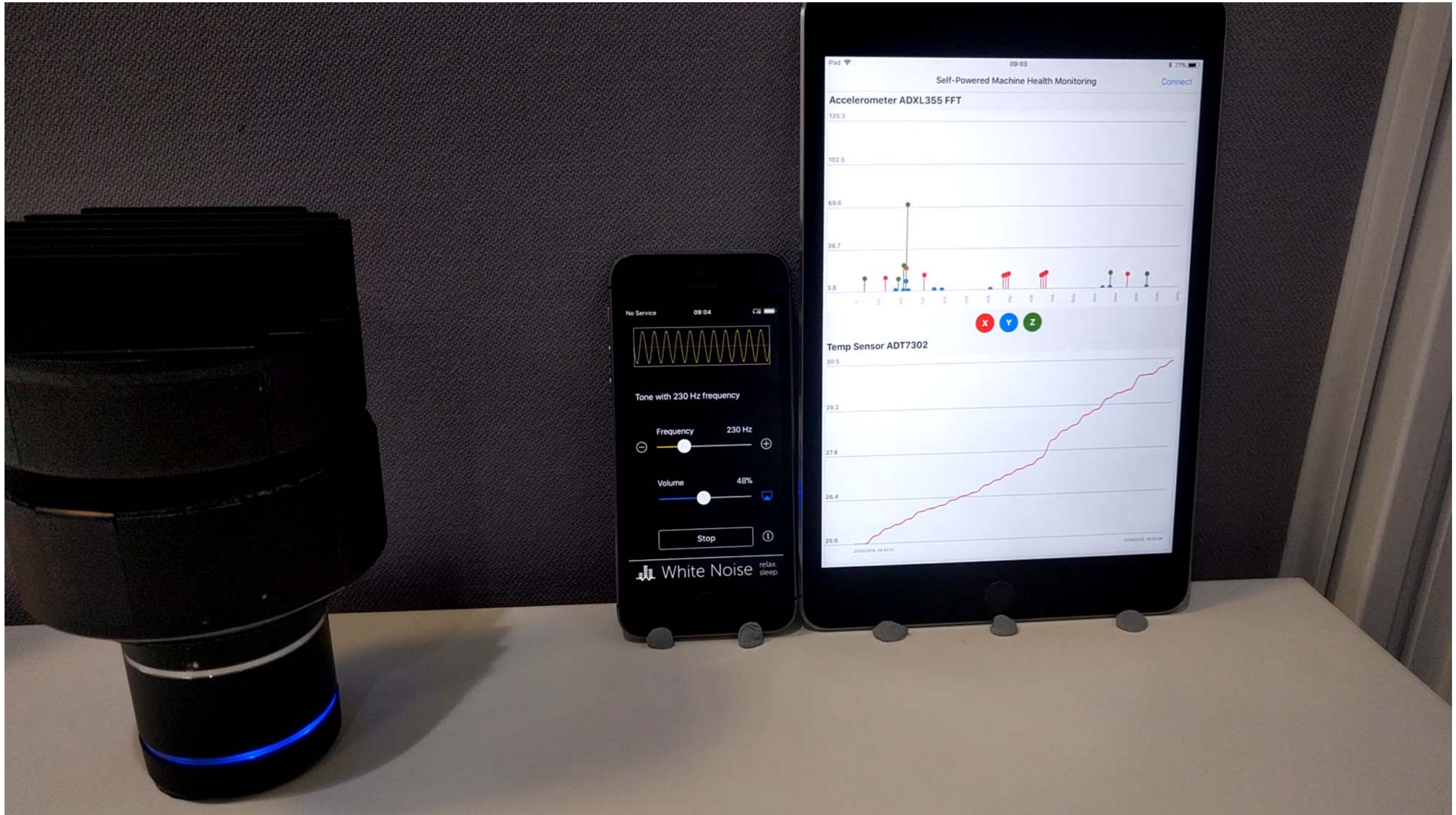


Heat flow



CbM Node

*Heat and
vibration
source*



TEG-Powered CbM Sensor Node

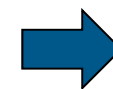
Average Power Consumption



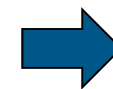
<i>Update rate</i>	DA14580 <i>BLE</i>	ADuCM3029 <i>uC</i>	ADXL355 <i>XL</i>	ADXL362 <i>Wake-up</i>	ADT7302 <i>Temp</i>	Total
30 sec	172	16.1	5.56	4.89	0.24	199
30 min	5.82	0.433	0.093	5.39	0.004	11.7

Average power in μW

- **Data updates every 30 sec:** Power consumption dominated by transmission
- **Data updates every 30 min:** Wake-up XL power consumption comparable to BLE

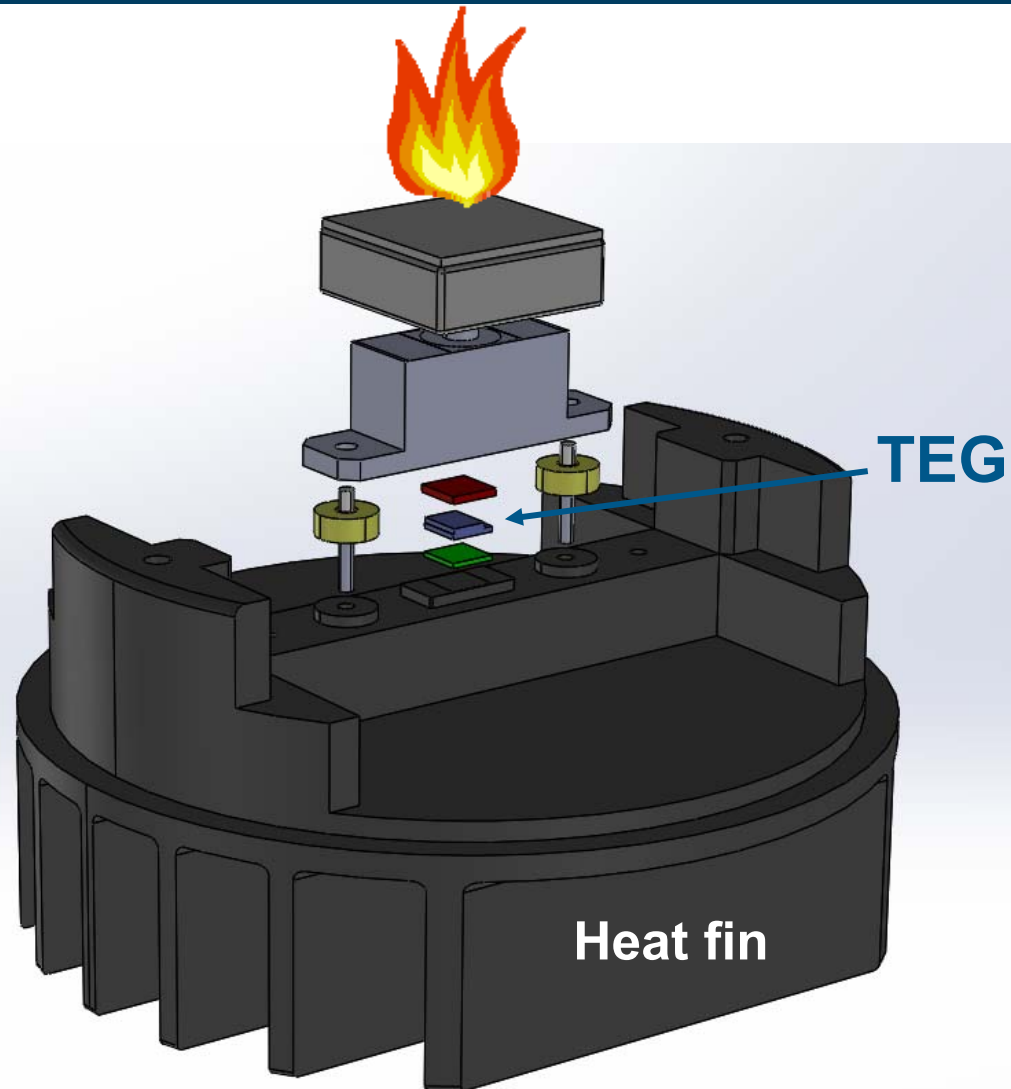


$\Delta T \sim 10^{\circ}\text{C}$



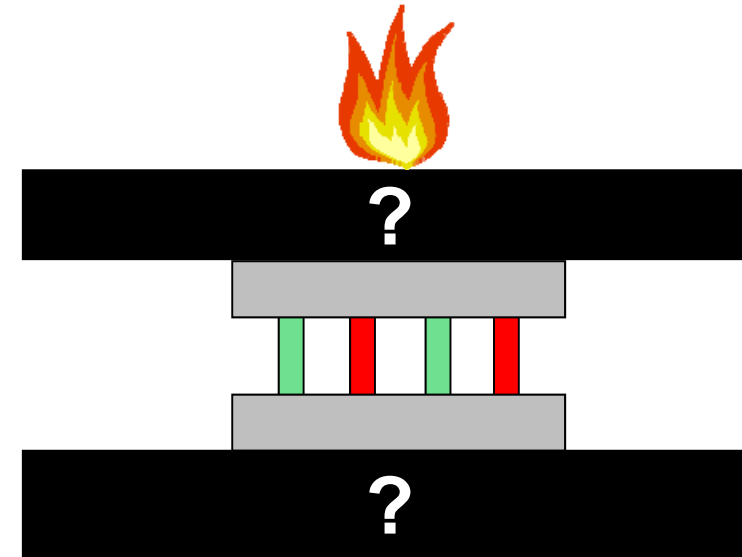
$\Delta T \sim 2^{\circ}\text{C}$

Thermal Breakdown



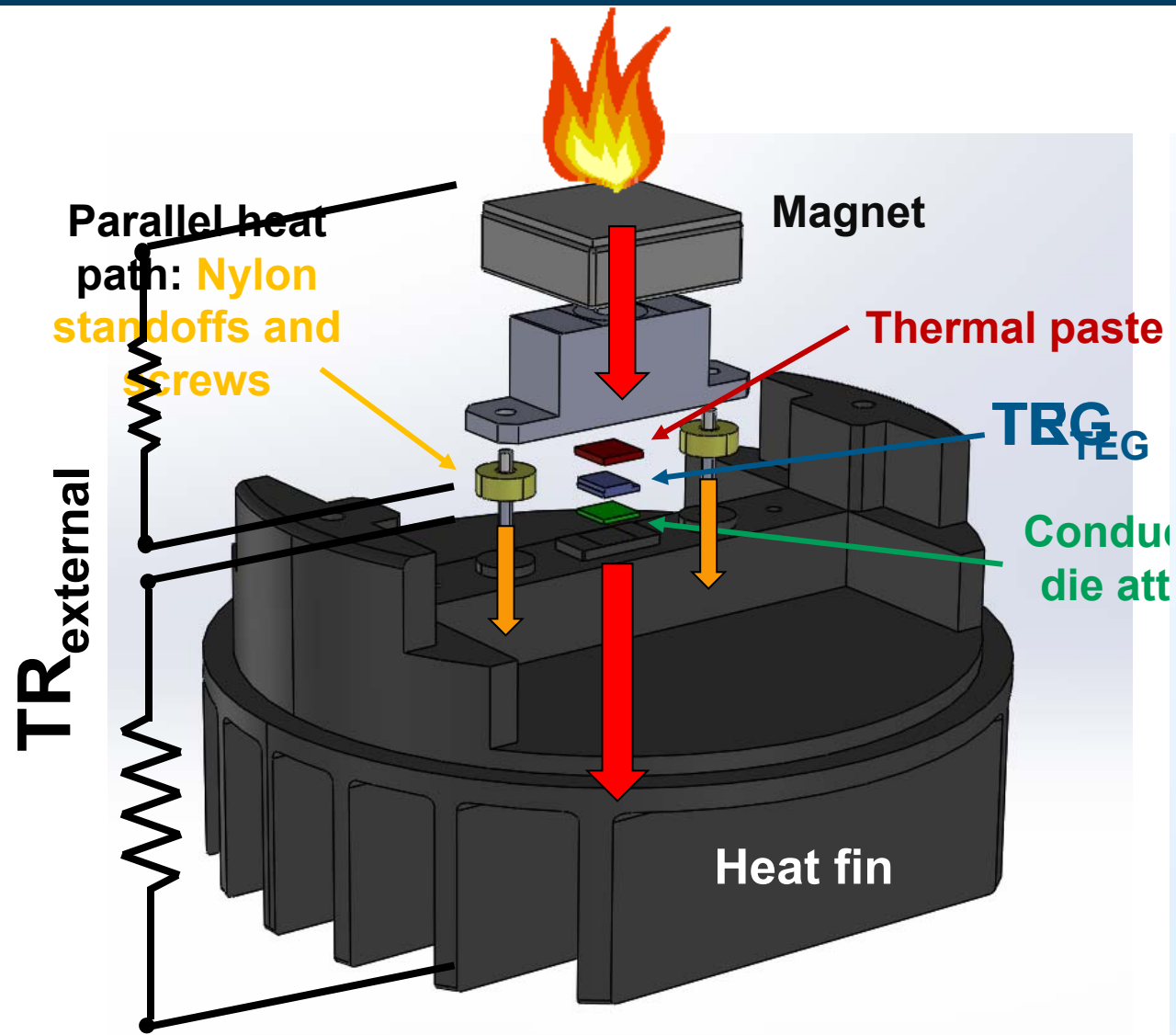
PCB and plastic housing not shown

Heat source



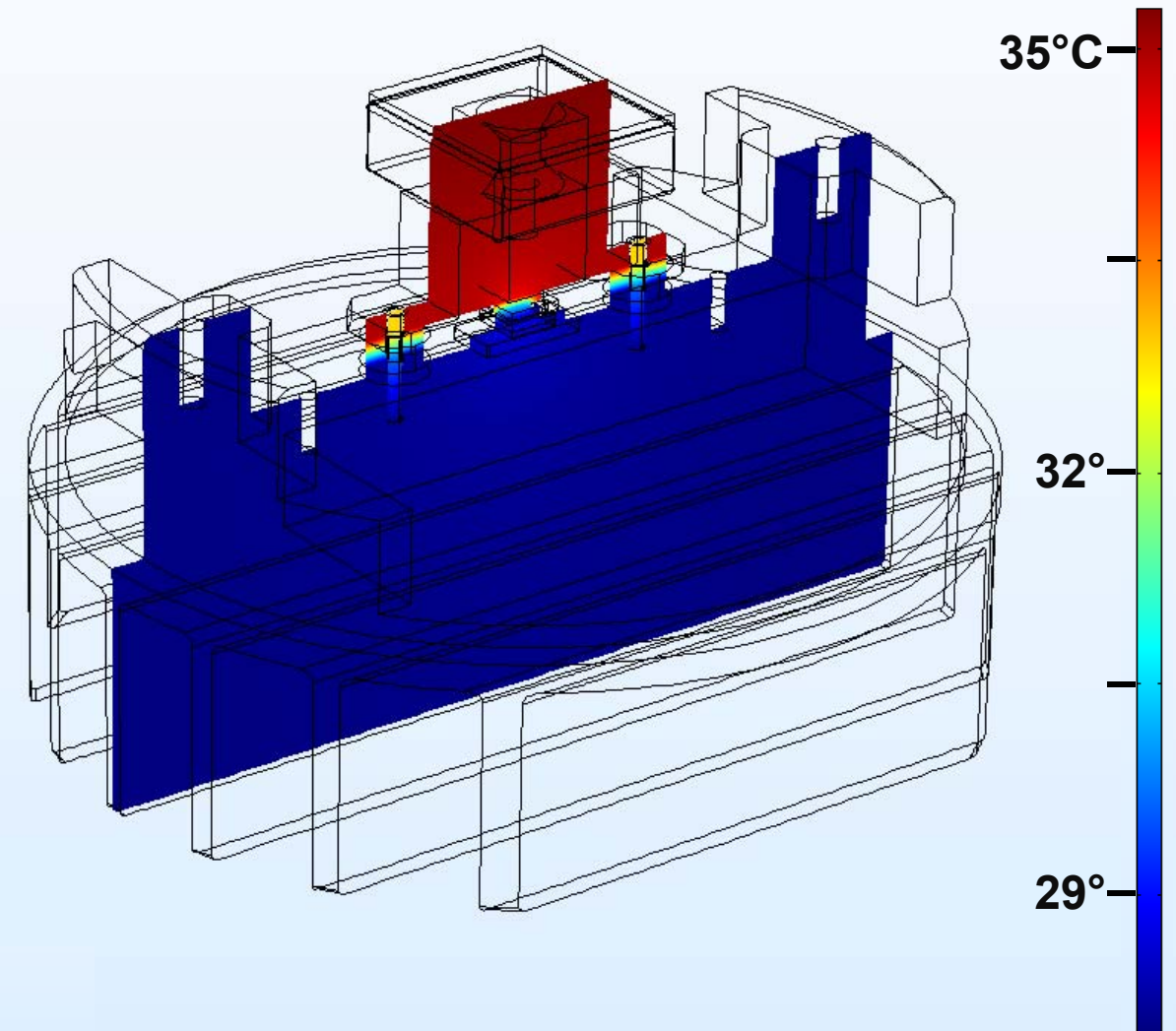
Heat sink


Thermal Breakdown



PCB and plastic housing not shown

Modeled Temperature Profile



- ▶ **Introduction to thermoelectricity**
 - *Make use of fundamental materials property*
 - *Can be used to heat/cool (input current) or to generate power (input ΔT)*
 - *Device efficiency related to TE material ZT*
- ▶ **Thermoelectric energy harvesting: Chip-scale technology offers significant advantages over typical bulk solutions**
- ▶ **TEG design and modeling**
 - *A lot can be learned from simple 1D models*
 - *Key device design requirement: Thermal impedance matching*
- ▶ **ADI chip-scale TEG**
 - *Based on patented device architecture: TE material deposited along polyimide slope*
 - *Large thermal resistance: Optimized for harvesting small amounts of energy from sources close to room temperature*
- ▶ **Condition-based monitoring sensor node: Smart sensing powered by TEG**
 -  *technology covers entire signal chain*

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